

16-bit Microcontroller

CMOS

F²MC-16LX MB90390 Series

MB90394HA/F394HA/F395HA/V390HB

■ DESCRIPTION

The MB90390-series with up to five FULL-CAN interfaces and Flash ROM is especially designed for automotive and industrial applications. Its main feature are up to five on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35 μ m CMOS technology, Fujitsu Microelectronics now offers on-chip Flash-ROM program memory up to 512 Kbytes. An internal voltage booster removes the necessity for a second programming voltage.

An on board voltage regulator provides 3 V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 41.7 ns instruction cycle time from an external 4 MHz clock.

The unit features 6 Stepper Motor Controllers with slew rate controlled high current outputs.

Furthermore it features an 8-channel Output Compare Unit and a 6-channel Input Capture Unit with two separate 16-bit Free Run Timers. Up to 4 UARTs constitute additional functionality for communication purposes.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevic.fujitsu.com/micom/en-support/>

■ FEATURES

- 16-bit core CPU; 4 MHz external clock (24 MHz internal, 41.7 ns instruction execution time)
- New 0.35 μ m CMOS Process Technology
- Internal voltage regulator supports 3 V MCU core, offering low EMI and low power consumption figures
- Up to five FULL-CAN interfaces; conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- Powerful interrupt functions (8 progr. priority levels; 8 external interrupts)
- EI²OS - Automatic transfer function indep.of CPU; 16 channels of intelligent I/O Services
- 18-bit Time-base counter
- Watchdog Timer
- 2 full duplex UARTs; support 10.4 Kbps (USA standard)
- Up to 2 full duplex UARTs (LIN/SCI)
- Serial I/O : 1 channel for synchronous data transfer
- Optional I²C with 400 Kbps
- A/D Converter : 15 channels analog inputs (Resolution 10 bits or 8 bits)
- 16-bit reload timer $\times$ 2 channels
- ICU (Input capture) 16-bit $\times$ 6 channels (2 input pins are shared with OCU outputs)
- OCU (Output capture) 16-bit $\times$ 8 channels (2 output pins are shared with ICU input pins)
- 16-bit Free Run Timer $\times$ 2 channels (FRT0 : ICU 0/1, OCU 0/1/2/3, FRT1 : ICU 2/3/4/5, OCU 4/5/6/7)
- 8/16-bit Programmable Pulse Generator 6 channels $\times$ 16-bit/12 channels $\times$ 8-bit
- Stepping Motor Controller 6 channels with slew rate controlled high current outputs
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- signed multiply (16-bit $\times$ 16-bit) and divide (32-bit/16-bit) instructions available
- Program Patch Function
- Fast Interrupt processing
- Low Power Consumption mode
 - Sleep mode
 - Timebase timer mode
 - Stop mode
 - CPU intermittent mode
- Sound Generator
- Real Time Watch Timer
- Built-In Clock Modulation circuit
- Programmable input levels (Automotive Hysteresis / CMOS Hysteresis, initial level is Automotive Hysteresis)
- Package : 120-pin plastic LQFP

■ PRODUCT LINEUP

Part Number Parameter	MB90394HA	MB90F394HA	MB90F395HA	MB90V390HB
CPU	F ² MC-16LX CPU			
System clock	On-chip PLL clock multiplier (× 1, × 2, × 3, × 4, × 6, 1/2 when PLL stops) Minimum instruction execution time : 41.7 ns (4 MHz osc. PLL × 6)			
ROM	ROM memory 384 Kbytes	Boot-block Flash memory 384 Kbytes Hard-wired reset vector, points to address FFA000 _H	Boot-block Flash memory 512 Kbytes Hard-wired reset vector, points to address FBA000 _H	External
RAM	10 Kbytes		30 Kbytes	
Emulator-specific power supply*1	—			Yes
Technology	0.35 μm CMOS with on-chip voltage regulator for internal power supply	0.35 μm CMOS with on-chip voltage regulator for internal power supply + Flash memory with On-chip charge pump for programming voltage		0.35 μm CMOS with on-chip voltage regulator for internal power supply
Operating voltage range	3.5 V to 5.5 V (4.0 V to 5.5 V: during Flash programming and erasing, 4.5 V to 5.5 V: if A/D Converter is used)			5 V ± 10%
Temperature range	−40 °C to +85 °C			—
Package	LQFP-120			PGA-299
UART (2 channels)	Full duplex double buffer Supports asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 24 MHz			
UART (LIN/SCI)	1 channel			2 channels
I ² C (400 Kbps)	1 channel	—	1 channel	
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 24 MHz			
A/D Converter	15 input channels 10-bit or 8-bit resolution Conversion time : Min 4.9 μs include sample time (per one channel, depends on machine clock frequency)			
16-bit Reload Timer (2 channels)	Operation clock frequency : fsys/2 ¹ , fsys/2 ³ , fsys/2 ⁵ (fsys = System clock frequency) Supports External Event Count function			

(Continued)

MB90390 Series

Part Number Parameter	MB90394HA	MB90F394HA	MB90F395HA	MB90V390HB
Watch Timer	Directly operates with the oscillation clock Read/Write accessible Second/Minute/Hour registers Signals interrupts			
16-bit Free Run Timer (2 channels)	Signals an interrupt when overflowing Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ , fsys/2 ⁵ , fsys/2 ⁶ , fsys/2 ⁷ (fsys = System clock freq.) Free Run Timer 0 (clock input FRCK0) corresponds to ICU 0/1, OCU 0/1/2/3 Free Run Timer 1 (clock input FRCK1) corresponds to ICU 2/3/4/5, OCU 4/5/6/7			
16-bit Output Compare (8 channels)	Signals an interrupt when a match with 16-bit Free Run Timer Eight 16-bit compare registers. A pair of compare registers can be used to generate an output signal. OCU 6/7 outputs are shared with ICU 3/5 inputs			
16-bit Input Capture (6 channels)	Rising edge, falling edge or rising & falling edge sensitive Six 16-bit Capture registers Signals an interrupt upon external event ICU 3/5 inputs are shared with OCU 6/7 outputs			
8/16-bit Programmable Pulse Generator (6 channels)	Supports 8-bit and 16-bit operation modes Twelve 8-bit reload counters Twelve 8-bit reload registers for L pulse width Twelve 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operation clock freq. : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ or 102.4 μ s at fosc = 5 MHz (fsys = System clock frequency, fosc = Oscillation clock frequency)			
CAN Interface (up to 5 channels)	2 channels			5 channels
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full-bit compare/Full-bit mask/Two partial bit masks Supports up to 1 Mbps			
Stepping Motor Controller (6 channels)	Four high current outputs with controlled slew rate for each channel Synchronized two 8-bit PWM's for each channel			
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive			
Sound Generator	8-bit PWM signal is mixed with tone frequency from 8-bit reload counter PWM frequency : 62.5 kHz, 31.2 kHz, 15.6 kHz, 7.8 kHz at System clock = 16 MHz Tone frequency : PWM frequency/2/ (reload value + 1)			

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Part Number Parameter	MB90394HA	MB90F394HA	MB90F395HA	MB90V390HB
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs Bit-wise programmable as input/output or peripheral signal Port-wise programmable as CMOS Hysteresis or automotive Hysteresis inputs (default)			
Clock Modulator	Spread spectrum clock modulator for reducing electromagnetic emissions. Frequency and Phase Modulation modes.			
Flash Memory	—	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 20 years*2 Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage		—

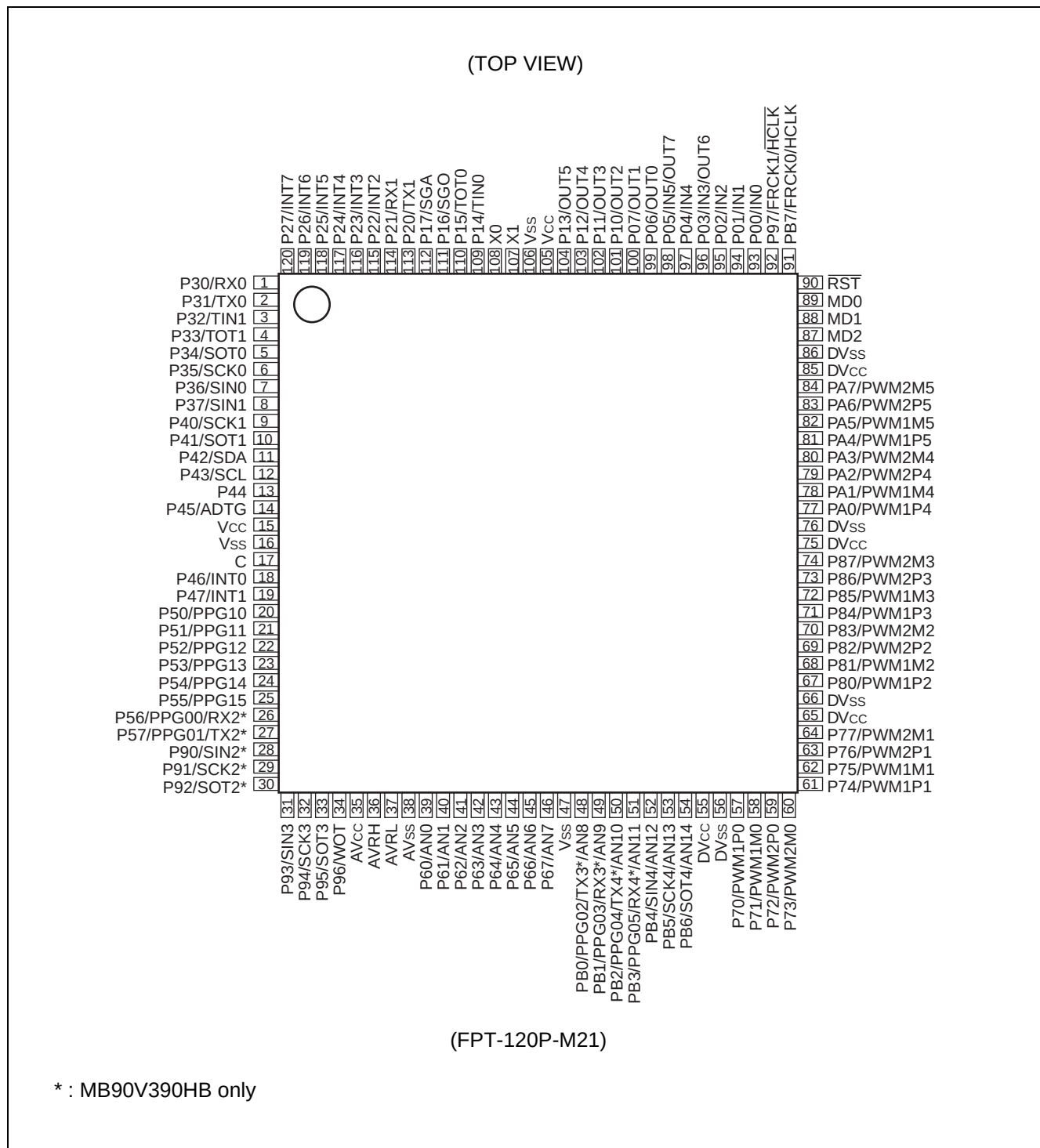
*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
 Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.

*2 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

MB90390 Series

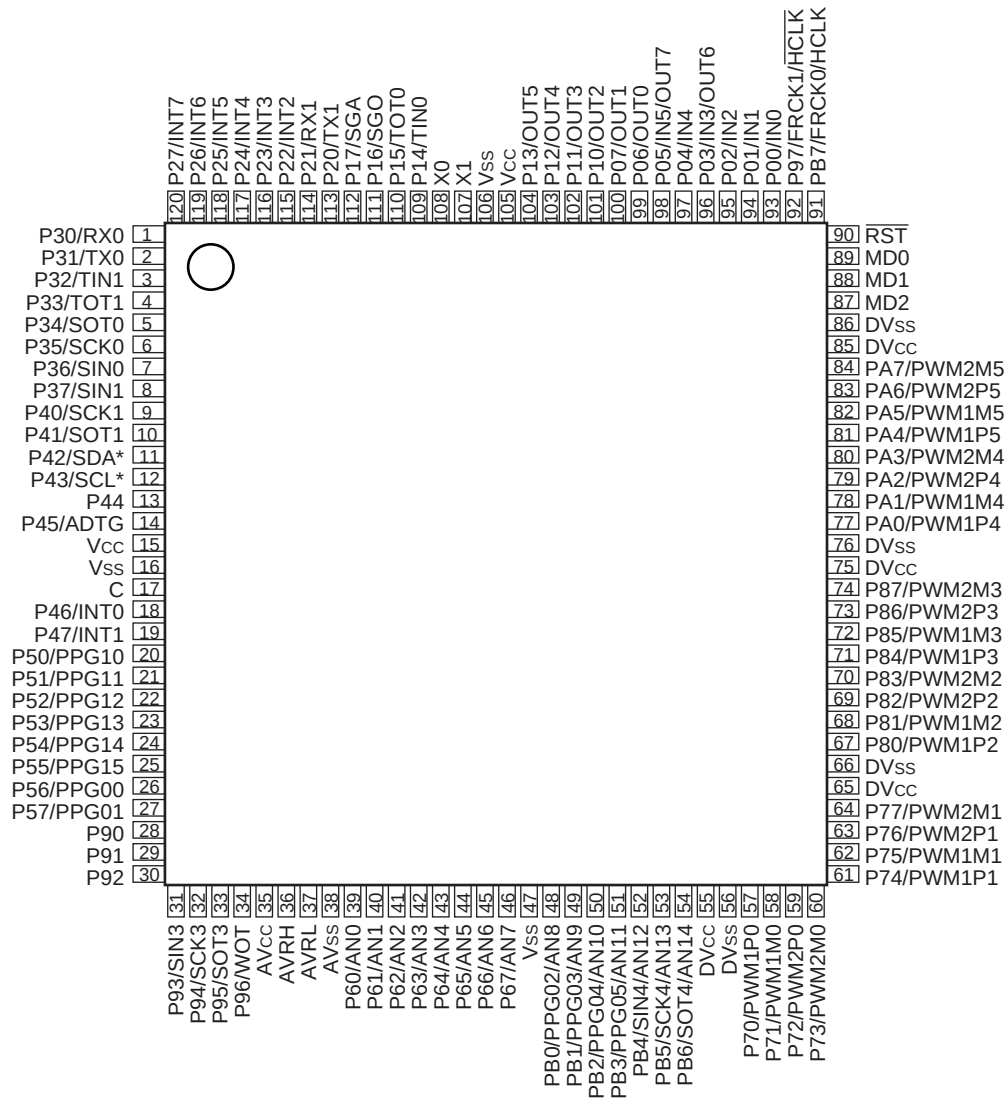
PIN ASSIGNMENTS

- MB90V390HB



- MB90394HA/MB90F394HA/MB90F395HA

(TOP VIEW)



(FPT-120P-M21)

* : These pins are not available in MB90F394HA.

MB90390 Series

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type*	Function
107	X1	A	Oscillation output
108	X0		Oscillation input
90	$\overline{\text{RST}}$	B	Reset input
93 to 95	P00 to P02	D	General purpose I/O
	IN0 to IN2		Inputs for the Input Captures 0 to 2
96	P03	D	General purpose I/O
	IN3		Input for the Input Capture 3
	OUT6		Output for the Output Compare 6
97	P04	D	General purpose I/O
	IN4		Input for the Input Capture 4
98	P05	D	General purpose I/O
	IN5		Input for the Input Capture 5
	OUT7		Output for the Output Compare 7
99 to 104	P06, P07, P10 to P13	D	General purpose I/O
	OUT0 to OUT5		Outputs for the Output Compares 0 to 5
109	P14	D	General purpose I/O
	TIN0		TIN0 input for the 16-bit Reload Timer 0
110	P15	D	General purpose I/O
	TOT0		TOT0 output for the 16-bit Reload Timer 0
111	P16	D	General purpose I/O
	SGO		SGO output for the Sound Generator
112	P17	D	General purpose I/O
	SGA		SGA output for the Sound Generator
113	P20	D	General purpose I/O
	TX1		TX output for CAN Interface 1
114	P21	D	General purpose I/O
	RX1		RX input for CAN Interface 1
115 to 120	P22 to P27	D	General purpose I/O
	INT2 to INT7		External interrupt inputs for INT2 to INT7
1	P30	D	General purpose I/O
	RX0		RX input for CAN Interface 0
2	P31	D	General purpose I/O
	TX0		TX output for CAN Interface 0

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Pin no.	Pin name	Circuit type*	Function
3	P32	D	General purpose I/O
	TIN1		TIN1 input for the 16-bit Reload Timer 1
4	P33	D	General purpose I/O
	TOT1		TOT1 output for the 16-bit Reload Timer 1
5	P34	D	General purpose I/O
	SOT0		SOT output for UART 0
6	P35	D	General purpose I/O
	SCK0		SCK I/O for UART 0
7	P36	D	General purpose I/O
	SIN0		SIN input for UART 0
8	P37	D	General purpose I/O
	SIN1		SIN input for UART 1
9	P40	D	General purpose I/O
	SCK1		SCK I/O for UART 1
10	P41	D	General purpose I/O
	SOT1		SOT output for UART 1
11	P42	D	General purpose I/O
	SDA		Serial data for I ² C interface (except MB90F394HA)
12	P43	D	General purpose I/O
	SCL		Serial clock for I ² C interface (except MB90F394HA)
13	P44	D	General purpose I/O
14	P45	D	General purpose I/O
	ADTG		External trigger input of the A/D Converter
18, 19	P46, P47	D	General purpose I/O
	INT0, INT1		External interrupt inputs for INT0 to INT1
20 to 25	P50 to P55	D	General purpose I/O
	PPG10 to PPG15		Outputs for the Programmable Pulse Generators 10 to 15
26	P56	D	General purpose I/O
	PPG00		Output for the Programmable Pulse Generator 0
	RX2		RX input for CAN Interface 2 (only MB90V390HB)
27	P57	D	General purpose I/O
	PPG01		Output for the Programmable Pulse Generator 1
	TX2		TX output for CAN Interface 2 (only MB90V390HB)
28	P90	D	General purpose I/O
	SIN2		SIN input for UART 2 (only MB90V390HB)

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MB90390 Series

Pin no.	Pin name	Circuit type*	Function
29	P91	D	General purpose I/O
	SCK2		SCK input/output for UART 2 (only MB90V390HB)
30	P92	D	General purpose I/O
	SOT2		SOT output for UART 2 (only MB90V390HB)
31	P93	D	General purpose I/O
	SIN3		SIN input for UART 3 (LIN/SCI)
32	P94	D	General purpose I/O
	SCK3		SCK input/output for UART 3 (LIN/SCI)
33	P95	D	General purpose I/O
	SOT3		SOT output for UART 3 (LIN/SCI)
34	P96	D	General purpose I/O
	WOT		WOT output for the Watch Timer
39 to 46	P60 to P67	E	General purpose I/O
	AN0 to AN7		Inputs for the A/D Converter
48	PB0	E	General purpose I/O
	PPG02		Output for the Programmable Pulse Generator 2
	TX3		TX output for CAN Interface 3 (only MB90V390HB)
	AN8		Input for the A/D Converter
49	PB1	E	General purpose I/O
	PPG03		Output for the Programmable Pulse Generator 3
	RX3		RX input for CAN Interface 3 (only MB90V390HB)
	AN9		Input for the A/D Converter
50	PB2	E	General purpose I/O
	PPG04		Output for the Programmable Pulse Generator 4
	TX4		TX output for CAN Interface 4 (only MB90V390HB)
	AN10		Input for the A/D Converter
51	PB3	E	General purpose I/O
	PPG05		Output for the Programmable Pulse Generator 5
	RX4		RX input for CAN Interface 4 (only MB90V390HB)
	AN11		Input for the A/D Converter
52	PB4	E	General purpose I/O
	SIN4		SIN input for the Serial I/O
	AN12		Input for the A/D Converter

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Pin no.	Pin name	Circuit type*	Function
53	PB5	E	General purpose I/O
	SCK4		SCK input/output for the Serial I/O
	AN13		Input for the A/D Converter
54	PB6	E	General purpose I/O
	SOT4		SOT output for the Serial I/O
	AN14		Input for the A/D Converter
57 to 60	P70 to P73	F	General purpose I/O
	PWM1P0 PWM1M0 PWM2P0 PWM2M0		Output for Stepping Motor Controller channel 0
61 to 64	P74 to P77	F	General purpose I/O
	PWM1P1 PWM1M1 PWM2P1 PWM2M1		Output for Stepping Motor Controller channel 1
67 to 70	P80 to P83	F	General purpose I/O
	PWM1P2 PWM1M2 PWM2P2 PWM2M2		Output for Stepping Motor Controller channel 2
71 to 74	P84 to P87	F	General purpose I/O
	PWM1P3 PWM1M3 PWM2P3 PWM2M3		Output for Stepping Motor Controller channel 3
77 to 80	PA0 to PA3	F	General purpose I/O
	PWM1P4 PWM1M4 PWM2P4 PWM2M4		Output for Stepping Motor Controller channel 4
81 to 84	PA4 to PA7	F	General purpose I/O
	PWM1P5 PWM1M5 PWM2P5 PWM2M5		Output for Stepping Motor Controller channel 5
91	PB7	D	General purpose I/O
	FRCK0		FRCK0 input for the 16-bit Free Run Timer 0
	HCLK		Oscillation Clock output

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MB90390 Series

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Pin no.	Pin name	Circuit type*	Function
92	P97	D	General purpose I/O
	FRCK1		FRCK1 input for the 16-bit Free Run Timer 1
	$\overline{\text{HCLK}}$		Inverted Oscillation Clock output
55 65 75 85	DVcc	—	Dedicated power supply pins for the high current output buffers (Pin No. 57 to 84)
56 66 76 86	DVss	—	Dedicated ground pins for the high current output buffers (Pin No. 57 to 84)
35	AVcc	—	Dedicated power supply pin (5 V) for the A/D converter
36	AVRH	—	Dedicated pos. reference voltage pin for the A/D converter
37	AVRL	—	Dedicated neg. reference voltage pin for the A/D converter
38	AVss	—	Dedicated power supply pin (0 V) for the A/D converter
88, 89	MD1, MD0	C	These are input pins used to designate the operating mode. They should be connected directly to Vcc or Vss.
87	MD2	G	This is an input pin used to designate the operating mode. It should be connected directly to Vcc or Vss.
15 105	Vcc	—	These are power supply (5 V) input pins
16 47 106	Vss	—	These are power supply (0 V) input pins
17	C	—	This is the power supply stabilization capacitor pin. It should be connected to higher than or equal to 0.1 μF (MB90394HA/ F394HA) / 0.22 μF (MB90F395HA/V390HB) ceramic capacitor.

* : Refer to "■ I/O CIRCUIT TYPE" for I/O circuit type.

I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation feedback resistor : 1 M Ω approx.
B		CMOS Hysteresis input with pull-up Resistor : 50 kΩ approx.
C		- EVA/ROM device : CMOS Hysteresis input - Flash device : CMOS input.
D		- CMOS output - CMOS Hysteresis input - Automotive Hysteresis input Note : The input characteristic may be different for different pins/devices. Refer to V_{IHS} in "■ ELECTRICAL CHARACTERISTICS 3.DC Characteristics"

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MB90390 Series

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Type	Circuit	Remarks
E	The circuit diagram for Type E shows a CMOS output stage with a P-channel MOSFET (P-ch) connected to V_{CC} and an N-channel MOSFET (N-ch) connected to ground. The gates of both transistors are connected to a common input node. Below this, there is an Analog input stage with a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch) connected to ground. The gates of these transistors are connected to a common input node. At the bottom, there are two hysteresis input stages. The first stage is labeled 'CMOS Hysteresis input' and consists of a resistor R connected to the input node and an inverter. The second stage is labeled 'Automotive Hysteresis input' and also consists of a resistor R connected to the input node and an inverter.	• CMOS output • CMOS Hysteresis input • Automotive Hysteresis input • Analog input Note : The input characteristic may be different for different pins/devices. Refer to V_{IHS} in "■ ELECTRICAL CHARACTERISTICS 3.DC Characteristics"
F	The circuit diagram for Type F shows a CMOS high current output stage with a P-channel MOSFET (P-ch) connected to DV_{CC} and an N-channel MOSFET (N-ch) connected to ground. The gates of both transistors are connected to a common input node. Below this, there are two hysteresis input stages. The first stage is labeled 'CMOS Hysteresis input' and consists of a resistor R connected to the input node and an inverter. The second stage is labeled 'Automotive Hysteresis input' and also consists of a resistor R connected to the input node and an inverter.	• CMOS high current output • CMOS Hysteresis input • Automotive Hysteresis input
G	The circuit diagram for Type G shows a CMOS Hysteresis input stage. It consists of a resistor R connected to the input node and an inverter. A pull-down resistor R (pull-down) is connected from the input node to ground.	• EVA/ROM device : CMOS Hysteresis input with pull-down Resistor : 50 kΩ approx. • Flash device : CMOS input without pull-down.

■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter if A/D Converter is unused.
- Notes on Energization
- Caution on Operations during PLL Clock Mode

1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC} , AV_{RH}) exceed the digital power-supply voltage.

2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.

For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

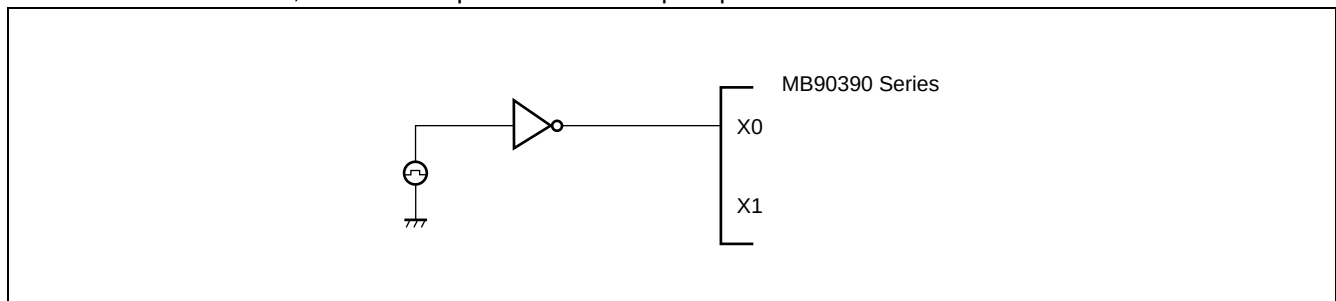
3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k Ω .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

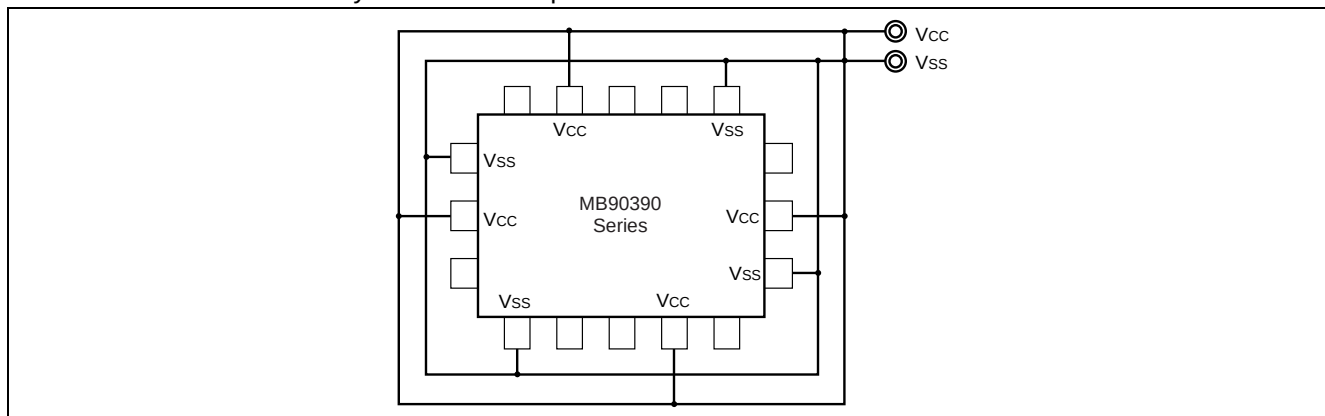
4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



5. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
- Connect V_{CC} and V_{SS} to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about $0.1\ \mu\text{F}$ as a bypass capacitor between V_{CC} and V_{SS} in the vicinity of V_{CC} and V_{SS} pins of the device.



6. Pull-up/down resistors

The MB90390 Series does not support internal pull-up/down resistors. Use external components where needed.

7. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

8. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , AV_{RH} , AV_{RL}) and analog inputs ($AN0$ to $AN14$) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed AV_{RH} or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

9. Connection of Unused Pins of A/D Converter if A/D Converter is unused

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$.

10. Notes on Energization

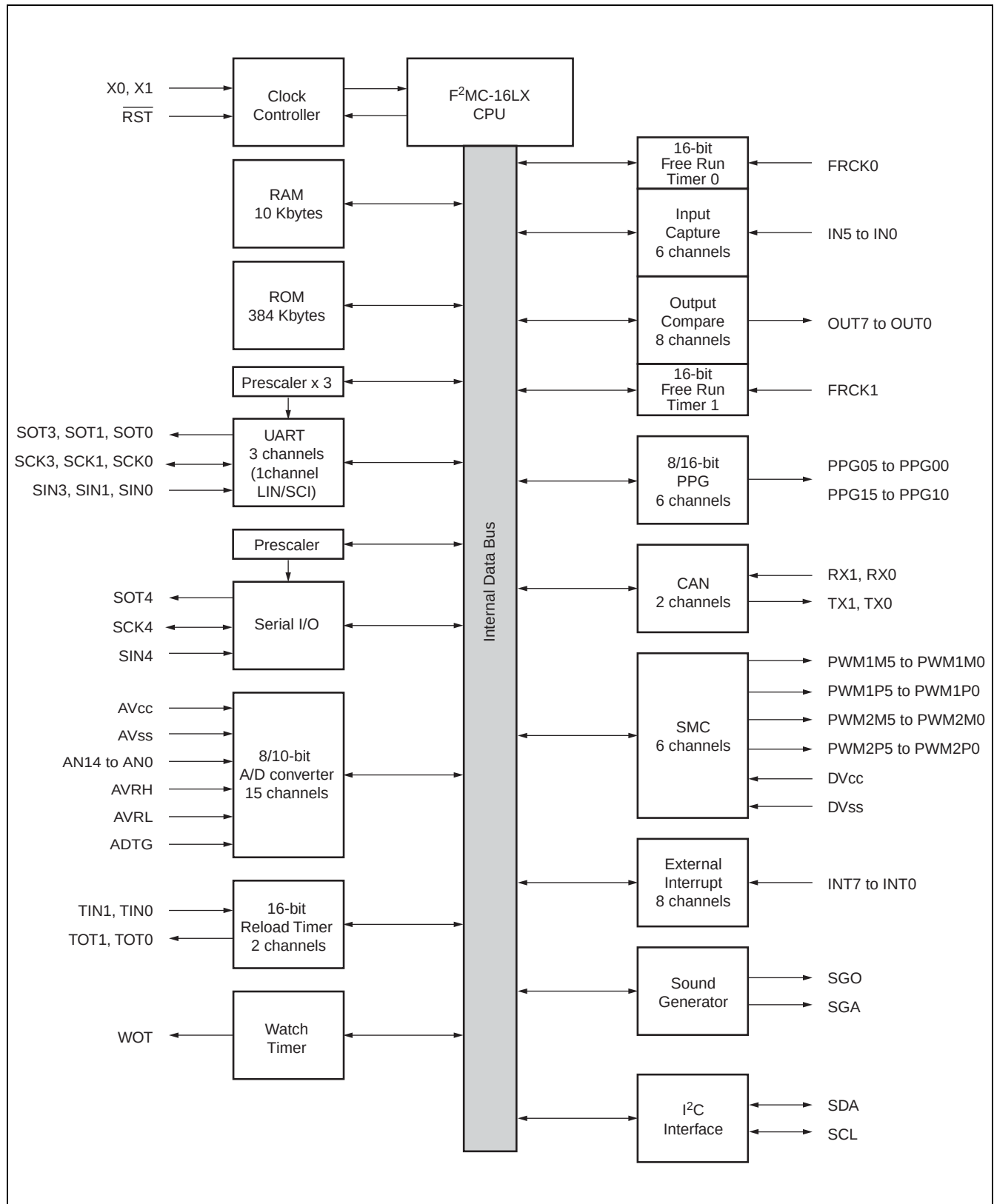
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 or more μs (0.2 V to 2.7 V).

11. Notes on During Operation of PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu Microelectronics will not guarantee results of operations if such failure occurs.

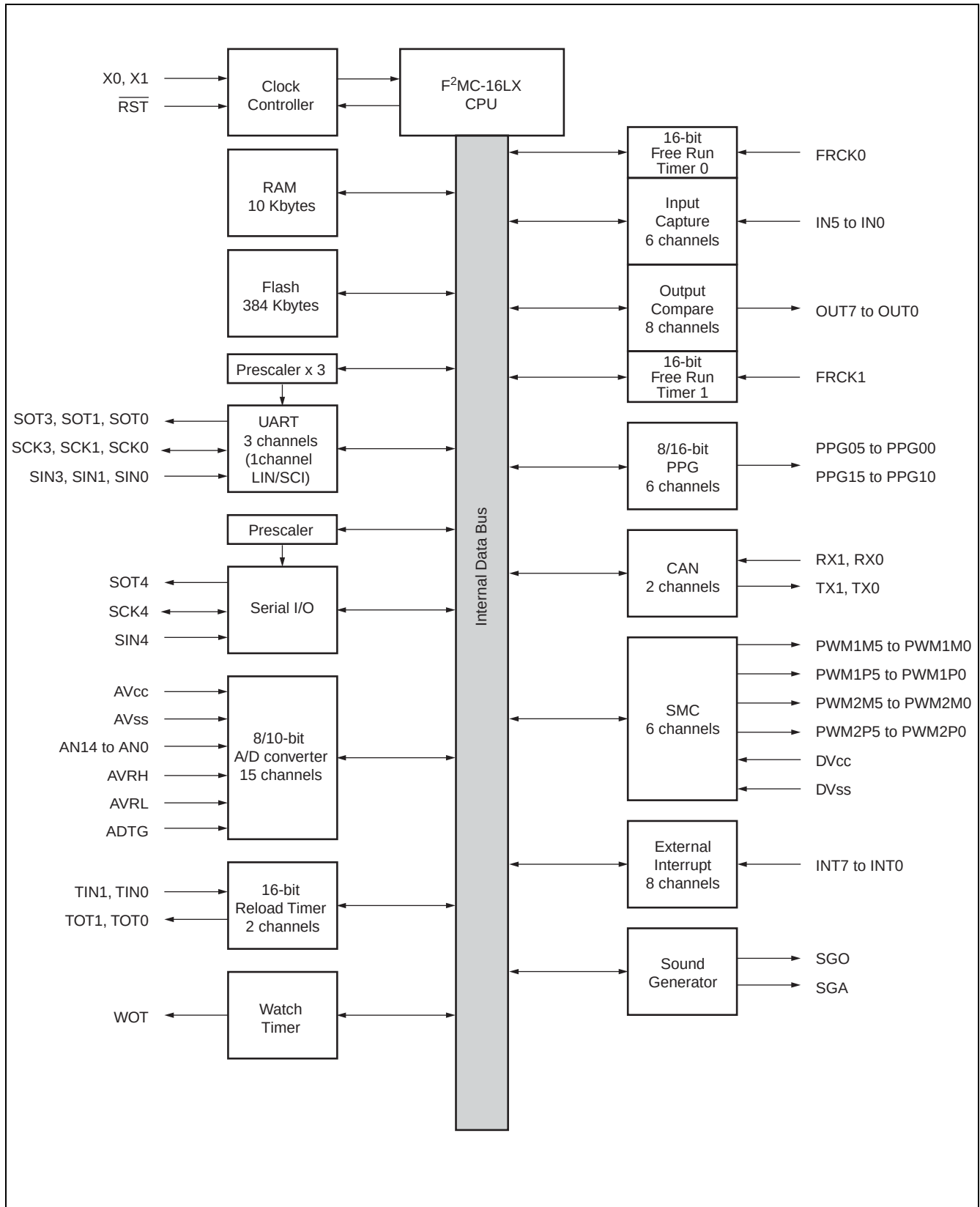
■ BLOCK DIAGRAMS

• MB90394HA

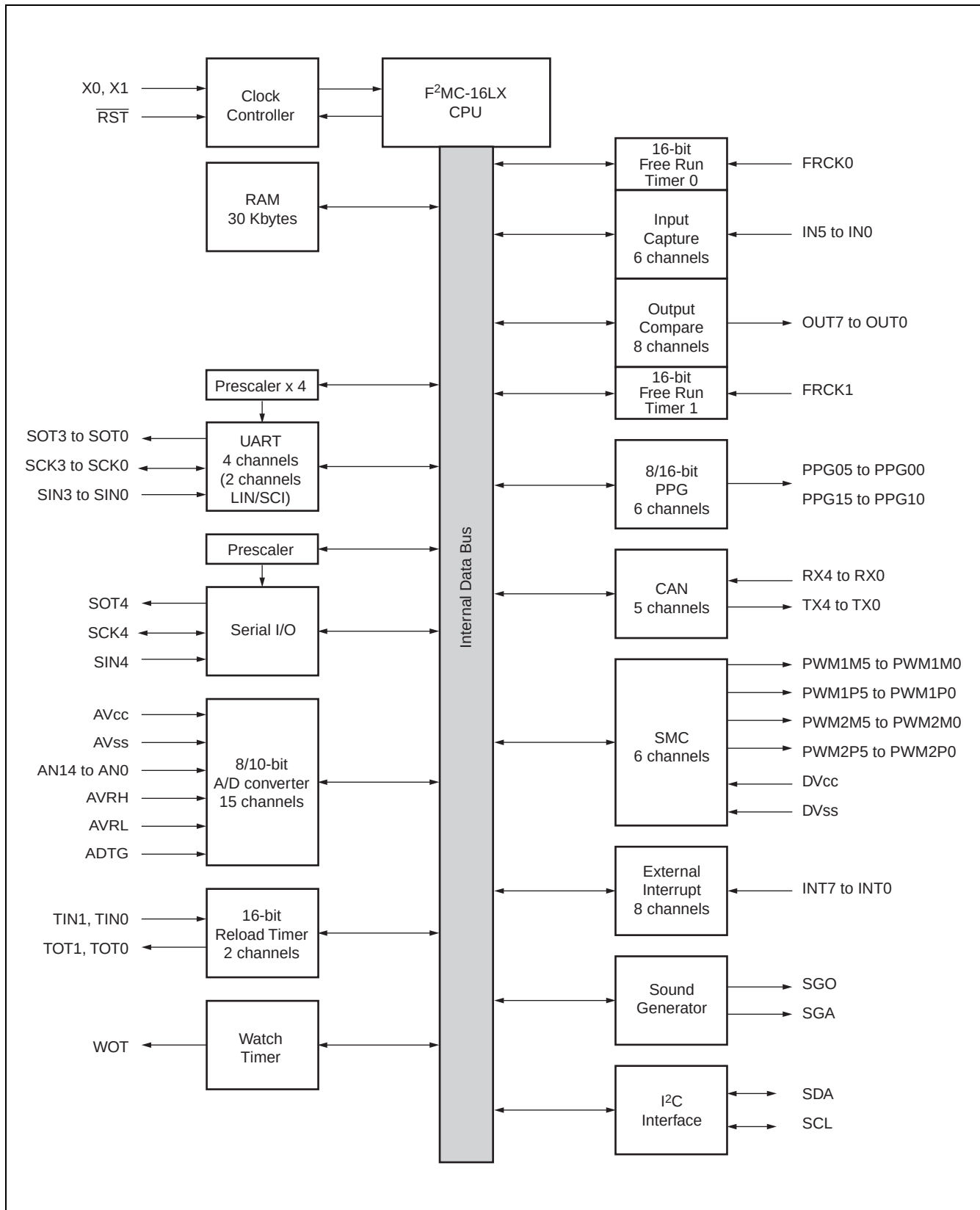


MB90390 Series

• MB90F394HA

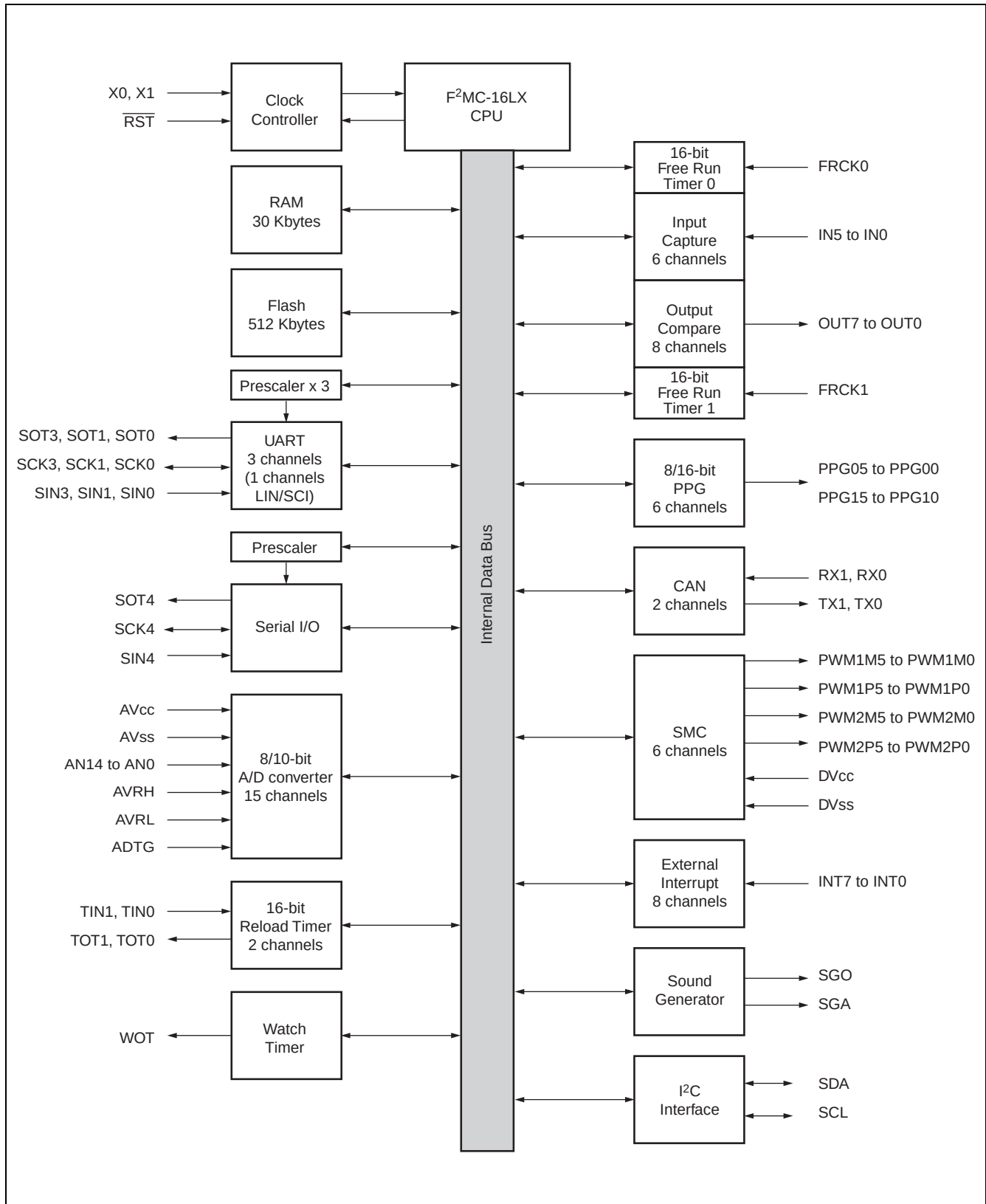


• MB90V390HB



MB90390 Series

• MB90F395HA



■ MEMORY MAP

MB90394HA/ MB90F394HA		MB90F395HA		MB90V390HB	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)
FF0000H		FF0000H		FF0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)
FE0000H		FE0000H		FE0000H	
FDFFFFH	ROM (FD bank)	FDFFFFH	ROM (FD bank)	FDFFFFH	ROM (FD bank)
FD0000H		FD0000H		FD0000H	
FCFFFFH		FCFFFFH	ROM (FC bank)	FCFFFFH	ROM (FC bank)
FC0000H		FC0000H		FC0000H	
FBFFFFH	ROM (FB bank)	FBFFFFH	ROM (FB bank)	FBFFFFH	ROM (FB bank)
FB0000H		FB0000H		FB0000H	
FAFFFFH	ROM (FA bank)	FAFFFFH	ROM (FA bank)	FAFFFFH	ROM (FA bank)
FA0000H		FA0000H		FA0000H	
F9FFFFH	ROM (F9 bank)	F9FFFFH	ROM (F9 bank)	F9FFFFH	ROM (F9 bank)
F90000H		F90000H		F90000H	
		F8FFFFH	ROM (F8 bank)	F8FFFFH	ROM (F8 bank)
		F80000H		F80000H	
		8017FFH	RAM 6 Kbytes	8017FFH	RAM 6 Kbytes
		800000H		800000H	
00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)
004000H or 008000H		008000H		008000H	
		0070FFH	RAM 12 Kbytes	0070FFH	RAM 12 Kbytes
		004100H		004100H	
003FFFFH	Periperal	003FFFFH	Periperal	003FFFFH	Periperal
003500H		003500H		003500H	
0028FFH		0030FFH		0030FFH	
	RAM 10 Kbytes		RAM 12 Kbytes		RAM 12 Kbytes
000100H		000100H		000100H	
0000BFH		0000BFH		0000BFH	
000000H	Periperal	000000H	Periperal	000000H	Periperal

Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.

For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.

The ROM area in bank FF exceeds 32/48 Kbytes, and its entire image cannot be shown in bank 00.

The image between FF4000H/FF8000H and FFFFFFFH is visible in bank 00, while the image between FF0000H and FF3FFFH/FF7FFFH is visible only in bank FF.

In MB90V390HB, the image for only ROM data between FF8000H to FFFFFFFH is visible in bank 00.

As for MB90394HA/F394HA/F395HA, it is possible to set the FF bank area which looks the 00 bank image in the ROM mirror function select register (ROMM) .

MB90390 Series

■ I/O MAP

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
00 _H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
01 _H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
02 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
03 _H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
04 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
05 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
06 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
07 _H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
08 _H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
09 _H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX _B
0A _H	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX _B
0B _H	Port B Data Register	PDRB	R/W	Port B	XXXXXXXX _B
0C _H	Analog Input Enable 0	ADER0	R/W	Port 6, A/D	11111111 _B
0D _H	Analog Input Enable 1/ ADC Select	ADER1	R/W	Port B, A/D	01111111 _B
0E _H	Input Level Select Register	ILSR	R/W	Ports	00000000 _B
0F _H	Input Level Select Register	ILSR	R/W	Ports	00000000 _B
10 _H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000 _B
11 _H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000 _B
12 _H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000 _B
13 _H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000 _B
14 _H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000 _B
15 _H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000 _B
16 _H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000 _B
17 _H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000 _B
18 _H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000 _B
19 _H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000 _B
1A _H	Port A Direction Register	DDRA	R/W	Port A	00000000 _B
1B _H	Port B Direction Register	DDRB	R/W	Port B	00000000 _B
1C _H to 1F _H	Reserved				
20 _H	Serial Mode Control 0	UMC0	R/W	UART0	00000100 _B
21 _H	Status 0	USR0	R/W		00010000 _B
22 _H	Input/Output Data 0	UIDR0/ UODR0	R/W		XXXXXXXX _B
23 _H	Rate and Data 0	URD0	R/W		0000000X _B

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
24 _H	Serial Mode Control 1	UMC1	R/W	UART1	00000100 _B
25 _H	Status 1	USR1	R/W		00010000 _B
26 _H	Input/Output Data 1	UIDR1/ UODR1	R/W		XXXXXXXX _B
27 _H	Rate and Data 1	URD1	R/W		0000000X _B
28 _H to 2B _H	Reserved				
2C _H	Serial Mode Control 4	SMCS4	R/W	Serial I/O	XXXX0000 _B
2D _H	Serial Mode Control 4	SMCS4	R/W		00000010 _B
2E _H	Serial Data 4	SDR4	R/W		XXXXXXXX _B
2F _H	Serial I/O Prescaler/Edge Selector 4	CDCR4	R/W		0X0X0000 _B
30 _H	External Interrupt Enable	ENIR	R/W	External Interrupt	00000000 _B
31 _H	External Interrupt Request	EIRR	R/W		XXXXXXXX _B
32 _H	External Interrupt Level	ELVR	R/W		00000000 _B
33 _H	External Interrupt Level	ELVR	R/W		00000000 _B
34 _H	A/D Control Status 0	ADCS0	R/W	A/D Converter	00000000 _B
35 _H	A/D Control Status 1	ADCS1	R/W		00000000 _B
36 _H	A/D Data 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D Data 1	ADCR1	R/W		000010XX _B
38 _H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0X000XX1 _B
39 _H	PPG1 Operation Mode Control Register	PPGC1	R/W		0X000001 _B
3A _H	PPG0 and PPG1 Clock Select Register	PPG01	R/W		000000XX _B
3B _H	Address Detection Control Register 1	PACSR1	R/W	Address Match Detection Function 1	00000000 _B
3C _H	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0X000XX1 _B
3D _H	PPG3 Operation Mode Control Register	PPGC3	R/W		0X000001 _B
3E _H	PPG2 and PPG3 Clock Select Register	PPG23	R/W		000000XX _B
3F _H	Clock Output Enable Register	CKOE	R/W	Clock Output	XXXXXX00 _B
40 _H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0X000XX1 _B
41 _H	PPG5 Operation Mode Control Register	PPGC5	R/W		0X000001 _B
42 _H	PPG4 and PPG5 Clock Select Register	PPG45	R/W		000000XX _B
43 _H	Reserved				
44 _H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1 _B
45 _H	PPG7 Operation Mode Control Register	PPGC7	R/W		0X000001 _B
46 _H	PPG6 and PPG7 Clock Select Register	PPG67	R/W		000000XX _B

(Continued)

MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
47 _H	Reserved				
48 _H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1 _B
49 _H	PPG9 Operation Mode Control Register	PPGC9	R/W		0X000001 _B
4A _H	PPG8 and PPG9 Clock Select Register	PPG89	R/W		000000XX _B
4B _H	Reserved				
4C _H	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0X000XX1 _B
4D _H	PPGB Operation Mode Control Register	PPGCB	R/W		0X000001 _B
4E _H	PPGA and PPGB Clock Select Register	PPGAB	R/W		000000XX _B
4F _H	Reserved				
50 _H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 _B
51 _H	Timer Control Status 0	TMCSR0	R/W		XXXXX0000 _B
52 _H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 _B
53 _H	Timer Control Status 1	TMCSR1	R/W		XXXXX0000 _B
54 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
55 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
56 _H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B
57 _H	Reserved				
58 _H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 _B
59 _H	Output Compare Control Status 1	OCS1	R/W		0XX00000 _B
5A _H	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 _B
5B _H	Output Compare Control Status 3	OCS3	R/W		0XX00000 _B
5C _H	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
5D _H	Output Compare Control Status 5	OCS5	R/W		0XX00000 _B
5E _H	Sound Control	SGCR	R/W	Sound Generator	00000000 _B
5F _H	Sound Control	SGCR	R/W		0XXXXXX0 _B
60 _H	Watch Timer Control	WTCR	R/W	Watch Timer	000XX000 _B
61 _H	Watch Timer Control	WTCR	R/W		00000000 _B
62 _H	PWM Control 0	PWC0	R/W	Stepping Motor Controller 0	00000XX0 _B
63 _H	Reserved				
64 _H	PWM Control 1	PWC1	R/W	Stepping Motor Controller 1	00000XX0 _B
65 _H	Reserved				
66 _H	PWM Control 2	PWC2	R/W	Stepping Motor Controller 2	00000XX0 _B
67 _H	Reserved				

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
68 _H	PWM Control 3	PWC3	R/W	Stepping Motor Controller 3	00000XX0 _B
69 _H	Reserved				
6A _H	PWM Control 4	PWC4	R/W	Stepping Motor Controller 4	00000XX0 _B
6B _H	Reserved				
6C _H	PWM Control 5	PWC5	R/W	Stepping Motor Controller 5	00000XX0 _B
6D _H	Reserved				
6E _H	Reserved				
6F _H	ROM Mirror	ROMM	W	ROM Mirror	XXXXXXXX1 _B
70 _H to 8F _H	Reserved for CAN Interface 0/1. Refer to “■ CAN CONTROLLERS”				
90 _H to 9D _H	Reserved				
9E _H	Address Detection Control Register 0	PACSR0	R/W	Address Match Detection Function 0	00000000 _B
9F _H	Delayed Interrupt/Release	DIRR	R/W	Delayed Interrupt	XXXXXXXX0 _B
A0 _H	Low-power Mode	LPMCR	R/W	Low Power Controller	00011000 _B
A1 _H	Clock Selector	CKSCR	R/W	Low Power Controller	11111100 _B
A2 _H to A7 _H	Reserved				
A8 _H	Watchdog Control	WDTC	R/W	Watchdog Timer	XXXXX111 _B
A9 _H	Time Base Timer Control	TBTC	R/W	Time Base Timer	1XX00100 _B
AA _H to AD _H	Reserved				
AE _H	Flash Control Status (Flash devices only. Otherwise reserved)	FMCS	R/W	Flash Memory	000X0XX0 _B
AF _H	Reserved				
B0 _H	Interrupt Control Register 00	ICR00	R/W	Interrupt Controller	00000111 _B
B1 _H	Interrupt Control Register 01	ICR01	R/W		00000111 _B
B2 _H	Interrupt Control Register 02	ICR02	R/W		00000111 _B
B3 _H	Interrupt Control Register 03	ICR03	R/W		00000111 _B
B4 _H	Interrupt Control Register 04	ICR04	R/W		00000111 _B
B5 _H	Interrupt Control Register 05	ICR05	R/W		00000111 _B
B6 _H	Interrupt Control Register 06	ICR06	R/W		00000111 _B
B7 _H	Interrupt Control Register 07	ICR07	R/W		00000111 _B
B8 _H	Interrupt Control Register 08	ICR08	R/W		00000111 _B
B9 _H	Interrupt Control Register 09	ICR09	R/W		00000111 _B

(Continued)

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Address	Register	Abbrevia- tion	Access	Resource name	Initial value
BA _H	Interrupt Control Register 10	ICR10	R/W	Interrupt Controller	00000111 _B
BB _H	Interrupt Control Register 11	ICR11	R/W		00000111 _B
BC _H	Interrupt Control Register 12	ICR12	R/W		00000111 _B
BD _H	Interrupt Control Register 13	ICR13	R/W		00000111 _B
BE _H	Interrupt Control Register 14	ICR14	R/W		00000111 _B
BF _H	Interrupt Control Register 15	ICR15	R/W		00000111 _B
C0 _H to FF _H	Reserved				
3500 _H	Reload L	PRL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
3501 _H	Reload H	PRLH0	R/W		XXXXXXXX _B
3502 _H	Reload L	PRL1	R/W		XXXXXXXX _B
3503 _H	Reload H	PRLH1	R/W		XXXXXXXX _B
3504 _H	Reload L	PRL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
3505 _H	Reload H	PRLH2	R/W		XXXXXXXX _B
3506 _H	Reload L	PRL3	R/W		XXXXXXXX _B
3507 _H	Reload H	PRLH3	R/W		XXXXXXXX _B
3508 _H	Reload L	PRL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
3509 _H	Reload H	PRLH4	R/W		XXXXXXXX _B
350A _H	Reload L	PRL5	R/W		XXXXXXXX _B
350B _H	Reload H	PRLH5	R/W		XXXXXXXX _B
350C _H	Reload L	PRL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
350D _H	Reload H	PRLH6	R/W		XXXXXXXX _B
350E _H	Reload L	PRL7	R/W		XXXXXXXX _B
350F _H	Reload H	PRLH7	R/W		XXXXXXXX _B
3510 _H	Reload L	PRL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX _B
3511 _H	Reload H	PRLH8	R/W		XXXXXXXX _B
3512 _H	Reload L	PRL9	R/W		XXXXXXXX _B
3513 _H	Reload H	PRLH9	R/W		XXXXXXXX _B
3514 _H	Reload L	PRLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX _B
3515 _H	Reload H	PRLHA	R/W		XXXXXXXX _B
3516 _H	Reload L	PRLB	R/W		XXXXXXXX _B
3517 _H	Reload H	PRLHB	R/W		XXXXXXXX _B
3518 _H	Serial Mode Register	SMR3	R/W	UART3 (LIN/SCI)	00000000 _B
3519 _H	Serial Control Register	SCR3	R/W		00000000 _B
351A _H	Reception/Transmission Data Regis- ter	RDR3/ TDR3	R/W		00000000 _B

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
351B _H	Serial Status Register	SSR3	R/W	UART3 (LIN/SCI)	00001000 _B
351C _H	Extended Communication Control Reg.	ECCR3	R/W		000000XX _B
351D _H	Extended Status/Control Register	ESCR3	R/W		00000X00 _B
351E _H	Baud Rate Register 0	BGR03	R/W		00000000 _B
351F _H	Baud Rate Register 1	BGR13	R/W		00000000 _B
3520 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
3521 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
3522 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
3523 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
3524 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
3525 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
3526 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
3527 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
3528 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
3529 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
352A _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
352B _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
352C _H	Timer Data 0	TCDT0	R/W	16-bit Free Run Timer 0	00000000 _B
352D _H	Timer Data 0	TCDT0	R/W		00000000 _B
352E _H	Timer Control 0	TCCS0	R/W		00000000 _B
352F _H	Timer Control 0	TCCS0	R/W		0XXXXXXXX _B
3530 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
3531 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
3532 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
3533 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
3534 _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
3535 _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
3536 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
3537 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
3538 _H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
3539 _H	Output Compare 4	OCCP4	R/W		XXXXXXXX _B
353A _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
353B _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B

(Continued)

MB90390 Series

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
353C _H	Timer Data 1	TCDT1	R/W	16-bit Free Run Timer 1	00000000 _B
353D _H	Timer Data 1	TCDT1	R/W		00000000 _B
353E _H	Timer Control 1	TCCS1	R/W		00000000 _B
353F _H	Timer Control 1	TCCS1	R/W		0XXXXXXXX _B
3540 _H	Timer 0/Reload 0	TMR0/ TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX _B
3541 _H	Timer 0/Reload 0	TMR0/ TMRLR0	R/W		XXXXXXXX _B
3542 _H	Timer 1/Reload 1	TMR1/ TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX _B
3543 _H	Timer 1/Reload 1	TMR1/ TMRLR1	R/W		XXXXXXXX _B
3544 _H , 3545 _H	Reserved				
3546 _H	Frequency Data	SGFR	R/W	Sound Generator	XXXXXXXX _B
3547 _H	Amplitude Data	SGAR	R/W		XXXXXXXX _B
3548 _H	Decrement Grade	SGDR	R/W		XXXXXXXX _B
3549 _H	Tone Count	SGTR	R/W		XXXXXXXX _B
354A _H	Sub-second Data	WTBR	R/W	Watch Timer	XXXXXXXX _B
354B _H	Sub-second Data	WTBR	R/W		XXXXXXXX _B
354C _H	Sub-second Data	WTBR	R/W		XXXXXXXX _B
354D _H	Second Data	WTSR	R/W		XX000000 _B
354E _H	Minute Data	WTMR	R/W		XX000000 _B
354F _H	Hour Data	WTHR	R/W		XX000000 _B
3550 _H	PWM1 Compare 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX _B
3551 _H	PWM2 Compare 0	PWC20	R/W		XXXXXXXX _B
3552 _H	PWM1 Select 0	PWS10	R/W		00000000 _B
3553 _H	PWM2 Select 0	PWS20	R/W		X0000000 _B
3554 _H	PWM1 Compare 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX _B
3555 _H	PWM2 Compare 1	PWC21	R/W		XXXXXXXX _B
3556 _H	PWM1 Select 1	PWS11	R/W		00000000 _B
3557 _H	PWM2 Select 1	PWS21	R/W		X0000000 _B
3558 _H	PWM1 Compare 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX _B
3559 _H	PWM2 Compare 2	PWC22	R/W		XXXXXXXX _B
355A _H	PWM1 Select 2	PWS12	R/W		00000000 _B
355B _H	PWM2 Select 2	PWS22	R/W		X0000000 _B

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
355C _H	PWM1 Compare 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX _B
355D _H	PWM2 Compare 3	PWC23	R/W		XXXXXXXX _B
355E _H	PWM1 Select 3	PWS13	R/W		00000000 _B
355F _H	PWM2 Select 3	PWS23	R/W		X0000000 _B
3560 _H	PWM1 Compare 4	PWC14	R/W	Stepping Motor Controller 4	XXXXXXXX _B
3561 _H	PWM2 Compare 4	PWC24	R/W		XXXXXXXX _B
3562 _H	PWM1 Select 4	PWS14	R/W		00000000 _B
3563 _H	PWM2 Select 4	PWS24	R/W		X0000000 _B
3564 _H	PWM1 Compare 5	PWC15	R/W	Stepping Motor Controller 5	XXXXXXXX _B
3565 _H	PWM2 Compare 5	PWC25	R/W		XXXXXXXX _B
3566 _H	PWM1 Select 5	PWS15	R/W		00000000 _B
3567 _H	PWM2 Select 5	PWS25	R/W		X0000000 _B
3568 _H	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
3569 _H	Output Compare Control Status 7	OCS7	R/W		XXX00000 _B
356A _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
356B _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
356C _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
356D _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
356E _H	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXXX0 _B
356F _H	CAN RX/TX redirect register	CANSWR	R/W	CAN 0/1/2/3	XXXX0000 _B
3570 _H to 359F _H	For CAN Interface 2/3/4. Refer to “■ CAN CONTROLLERS”				
35A0 _H	I ² C Bus Status Register	IBSR	R	I ² C Interface* ³	00000000 _B
35A1 _H	I ² C Bus Control Register	IBCR	R/W		00000000 _B
35A2 _H	I ² C Ten Bit Slave Address Register	ITBAL	R/W		00000000 _B
35A3 _H		ITBAH	R/W		XXXXXX00 _B
35A4 _H	I ² C Ten Bit Address Mask Register	ITMKL	R/W		11111111 _B
35A5 _H		ITMKH	R/W		00XXXX11 _B
35A6 _H	I ² C Seven Bit Slave Address Register	ISBA	R/W		X0000000 _B
35A7 _H	I ² C Seven Bit Address Mask Register	ISMK	R/W		01111111 _B
35A8 _H	I ² C Data Register	IDAR	R/W		00000000 _B
35A9 _H	I ² C Noise Filter Configuration Register	INFCR	R/W		XXXXXX01 _B
35AA _H	Reserved				
35AB _H	I ² C Clock Control Register	ICCR	R/W	I ² C Interface* ³	X0011111 _B
35AC _H to 35BF _H	Reserved				
35C0 _H	Parameter Register Low Byte	CMPRL	R/W	Clock Modulator	11111101 _B

(Continued)

MB90390 Series

Address	Register	Abbreviation	Access	Resource name	Initial value
35C1 _H	Parameter Register High Byte	CMPRH	R/W	Clock Modulator	XX000010 _B
35C2 _H	Clock Modulator Control Register	CMCR	R/W		00010000 _B
35C3 _H to 35C8 _H	Reserved				
35C9 _H	Input Capture Edge 0/1	ICE01	R/W	Input Capture 0/1	XXXXXX0XX _B
35CA _H	Input Capture Edge 2/3*2	ICE23	R	Input Capture 2/3	XXXXXXXXXX _B
35CB _H	Input Capture Edge 4/5	ICE45	R/W	Input Capture 4/5	XXXXXX0XX _B
35CC _H to 35CE _H	Reserved				
35CF _H	PLL and special configuration control resister	PSCCR	W	PLL	XXXX0000 _B
35D0 _H to 35D7 _H	Reserved				
35D8 _H	Serial Mode Register	SMR2	R/W	UART2*1 (LIN/SCI)	00000000 _B
35D9 _H	Serial Control Register	SCR2	R/W		00000000 _B
35DA _H	Reception/Transmission Data Register	RDR2/ TDR2	R/W		00000000 _B
35DB _H	Serial Status Register	SSR2	R/W		00001000 _B
35DC _H	Extended Communication Control Register	ECCR2	R/W		000000XX _B
35DD _H	Extended Status/Control Register	ESCR2	R/W		00000X00 _B
35DE _H	Baud Rate Register 0	BGR02	R/W		00000000 _B
35DF _H	Baud Rate Register 1	BGR12	R/W		00000000 _B
35E0 _H	Detection Address Setting Register 0 (Low-order)	PADR0	R/W	Address Match Detection Function 0	XXXXXXXXXX _B
35E1 _H	Detection Address Setting Register 0 (Middle-order)	PADR0	R/W		XXXXXXXXXX _B
35E2 _H	Detection Address Setting Register 0 (High-order)	PADR0	R/W		XXXXXXXXXX _B
35E3 _H	Detection Address Setting Register 1 (Low-order)	PADR1	R/W		XXXXXXXXXX _B
35E4 _H	Detection Address Setting Register 1 (Middle-order)	PADR1	R/W		XXXXXXXXXX _B
35E5 _H	Detection Address Setting Register 1 (High-order)	PADR1	R/W		XXXXXXXXXX _B
35E6 _H to 35EF _H	Reserved				
35F0 _H	Detection Address Setting Register 3 (Low-order)	PADR3	R/W	Address Match Detection Function 1	XXXXXXXXXX _B
35F1 _H	Detection Address Setting Register 3 (Middle-order)	PADR3	R/W		XXXXXXXXXX _B

(Continued)

(Continued)

Address	Register	Abbrevia- tion	Access	Resource name	Initial value
35F2 _H	Detection Address Setting Register 3 (High-order)	PADR3	R/W	Address Match Detection Function 1	XXXXXXXX _B
35F3 _H	Detection Address Setting Register 4 (Low-order)	PADR4	R/W		XXXXXXXX _B
35F4 _H	Detection Address Setting Register 4 (Middle-order)	PADR4	R/W		XXXXXXXX _B
35F5 _H	Detection Address Setting Register 4 (High-order)	PADR4	R/W		XXXXXXXX _B
35F6 _H	Detection Address Setting Register 5 (Low-order)	PADR5	R/W		XXXXXXXX _B
35F7 _H	Detection Address Setting Register 5 (Middle-order)	PADR5	R/W		XXXXXXXX _B
35F8 _H	Detection Address Setting Register 5 (High-order)	PADR5	R/W		XXXXXXXX _B
35F9 _H to 35FF _H	Reserved				
3600 _H to 37FF _H	Area for CAN Interface 0. Refer to “  CAN CONTROLLERS”				
3800 _H to 39FF _H	Area for CAN Interface 1. Refer to “  CAN CONTROLLERS”				
3A00 _H to 3BFF _H	Area for CAN Interface 2. Refer to “  CAN CONTROLLERS”				
3C00 _H to 3DFF _H	Area for CAN Interface 3. Refer to “  CAN CONTROLLERS”				
3E00 _H to 3FFF _H	Area for CAN Interface 4. Refer to “  CAN CONTROLLERS”				

*1 : UART2 (LIN/SCI) is only available in MB90V390HB.

*2 : Input Capture Edge 2/3 register is different in MB90V390HB, the access is “R/W” and initial value is “XXXXX0XX_B”.

*3 : I²C Interface is not available in MB90F394HA.

MB90390 Series

- Explanation on read/write
R/W : Readable and writable
R : Read only
W : Write only
- Explanation on initial values
0 : Initial value is "0".
1 : Initial value is "1".
X : Initial value is undefined.

Note : Any write access to reserved addresses in I/O map should not be performed. A read access to reserved address results in reading "X".

■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance mask register 0/acceptance mask register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address					Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
000070 _H	000080 _H	003570 _H	003580 _H	003590 _H	Message buffer valid register	BVALR	R/W	00000000 _B 00000000 _B
000071 _H	000081 _H	003571 _H	003581 _H	003591 _H				
000072 _H	000082 _H	003572 _H	003582 _H	003592 _H	Transmit request register	TREQR	R/W	00000000 _B 00000000 _B
000073 _H	000083 _H	003573 _H	003583 _H	003593 _H				
000074 _H	000084 _H	003574 _H	003584 _H	003594 _H	Transmit cancel register	TCANR	W	00000000 _B 00000000 _B
000075 _H	000085 _H	003575 _H	003585 _H	003595 _H				
000076 _H	000086 _H	003576 _H	003586 _H	003596 _H	Transmit complete register	TCR	R/W	00000000 _B 00000000 _B
000077 _H	000087 _H	003577 _H	003587 _H	003597 _H				
000078 _H	000088 _H	003578 _H	003588 _H	003598 _H	Receive complete register	RCR	R/W	00000000 _B 00000000 _B
000079 _H	000089 _H	003579 _H	003589 _H	003599 _H				
00007A _H	00008A _H	00357A _H	00358A _H	00359A _H	Remote request receiving register	RRTRR	R/W	00000000 _B 00000000 _B
00007B _H	00008B _H	00357B _H	00358B _H	00359B _H				
00007C _H	00008C _H	00357C _H	00358C _H	00359C _H	Receive overrun register	ROVRR	R/W	00000000 _B 00000000 _B
00007D _H	00008D _H	00357D _H	00358D _H	00359D _H				
00007E _H	00008E _H	00357E _H	00358E _H	00359E _H	Receive interrupt enable register	RIER	R/W	00000000 _B 00000000 _B
00007F _H	00008F _H	00357F _H	00358F _H	00359F _H				

MB90390 Series

List of Control Registers (2)

Address					Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003700 _H	003900 _H	003B00 _H	003D00 _H	003F00 _H	Control status register	CSR	R/W, R	00XXX000 _B 0XXXX0X1 _B
003701 _H	003901 _H	003B01 _H	003D01 _H	003F01 _H				
003702 _H	003902 _H	003B02 _H	003D02 _H	003F02 _H	Last event indicator register	LEIR	R/W	XXXXXXXX _B 000X0000 _B
003703 _H	003903 _H	003B03 _H	003D03 _H	003F03 _H				
003704 _H	003904 _H	003B04 _H	003D04 _H	003F04 _H	Receive/transmit error counter	RTEC	R	00000000 _B 00000000 _B
003705 _H	003905 _H	003B05 _H	003D05 _H	003F05 _H				
003706 _H	003906 _H	003B06 _H	003D06 _H	003F06 _H	Bit timing register	BTR	R/W	X1111111 _B 11111111 _B
003707 _H	003907 _H	003B07 _H	003D07 _H	003F07 _H				
003708 _H	003908 _H	003B08 _H	003D08 _H	003F08 _H	IDE register	IDER	R/W	XXXXXXXX _B XXXXXXXX _B
003709 _H	003909 _H	003B09 _H	003D09 _H	003F09 _H				
00370A _H	00390A _H	003B0A _H	003D0A _H	003F0A _H	Transmit RTR register	TRTRR	R/W	00000000 _B 00000000 _B
00370B _H	00390B _H	003B0B _H	003D0B _H	003F0B _H				
00370C _H	00390C _H	003B0C _H	003D0C _H	003F0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX _B XXXXXXXX _B
00370D _H	00390D _H	003B0D _H	003D0D _H	003F0D _H				
00370E _H	00390E _H	003B0E _H	003D0E _H	003F0E _H	Transmit interrupt enable register	TIER	R/W	00000000 _B 00000000 _B
00370F _H	00390F _H	003B0F _H	003D0F _H	003F0F _H				
003710 _H	003910 _H	003B10 _H	003D10 _H	003F10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX _B XXXXXXXX _B
003711 _H	003911 _H	003B11 _H	003D11 _H	003F11 _H				
003712 _H	003912 _H	003B12 _H	003D12 _H	003F12 _H				XXXXXXXX _B XXXXXXXX _B
003713 _H	003913 _H	003B13 _H	003D13 _H	003F13 _H				
003714 _H	003914 _H	003B14 _H	003D14 _H	003F14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX _B XXXXXXXX _B
003715 _H	003915 _H	003B15 _H	003D15 _H	003F15 _H				
003716 _H	003916 _H	003B16 _H	003D16 _H	003F16 _H				XXXXXXXX _B XXXXXXXX _B
003717 _H	003917 _H	003B17 _H	003D17 _H	003F17 _H				
003718 _H	003918 _H	003B18 _H	003D18 _H	003F18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX _B XXXXXXXX _B
003719 _H	003919 _H	003B19 _H	003D19 _H	003F19 _H				
00371A _H	00391A _H	003B1A _H	003D1A _H	003F1A _H				XXXXXXXX _B XXXXXXXX _B
00371B _H	00391B _H	003B1B _H	003D1B _H	003F1B _H				

List of Message Buffers (ID Registers) (1)

Address					Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003600 _H to 00361F _H	003800 _H to 00381F _H	003A00 _H to 003A1F _H	003C00 _H to 003C1F _H	003E00 _H to 003E1F _H	General- purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003620 _H	003820 _H	003A20 _H	003C20 _H	003E20 _H	ID register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
003621 _H	003821 _H	003A21 _H	003C21 _H	003E21 _H				XXXXXXXX _B XXXXXXXX _B
003622 _H	003822 _H	003A22 _H	003C22 _H	003E22 _H				XXXXXXXX _B XXXXXXXX _B
003623 _H	003823 _H	003A23 _H	003C23 _H	003E23 _H				XXXXXXXX _B XXXXXXXX _B
003624 _H	003824 _H	003A24 _H	003C24 _H	003E24 _H	ID register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
003625 _H	003825 _H	003A25 _H	003C25 _H	003E25 _H				XXXXXXXX _B XXXXXXXX _B
003626 _H	003826 _H	003A26 _H	003C26 _H	003E26 _H				XXXXXXXX _B XXXXXXXX _B
003627 _H	003827 _H	003A27 _H	003C27 _H	003E27 _H				XXXXXXXX _B XXXXXXXX _B
003628 _H	003828 _H	003A28 _H	003C28 _H	003E28 _H	ID register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
003629 _H	003829 _H	003A29 _H	003C29 _H	003E29 _H				XXXXXXXX _B XXXXXXXX _B
00362A _H	00382A _H	003A2A _H	003C2A _H	003E2A _H				XXXXXXXX _B XXXXXXXX _B
00362B _H	00382B _H	003A2B _H	003C2B _H	003E2B _H				XXXXXXXX _B XXXXXXXX _B
00362C _H	00382C _H	003A2C _H	003C2C _H	003E2C _H	ID register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
00362D _H	00382D _H	003A2D _H	003C2D _H	003E2D _H				XXXXXXXX _B XXXXXXXX _B
00362E _H	00382E _H	003A2E _H	003C2E _H	003E2E _H				XXXXXXXX _B XXXXXXXX _B
00362F _H	00382F _H	003A2F _H	003C2F _H	003E2F _H				XXXXXXXX _B XXXXXXXX _B
003630 _H	003830 _H	003A30 _H	003C30 _H	003E30 _H	ID register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
003631 _H	003831 _H	003A31 _H	003C31 _H	003E31 _H				XXXXXXXX _B XXXXXXXX _B
003632 _H	003832 _H	003A32 _H	003C32 _H	003E32 _H				XXXXXXXX _B XXXXXXXX _B
003633 _H	003833 _H	003A33 _H	003C33 _H	003E33 _H				XXXXXXXX _B XXXXXXXX _B
003634 _H	003834 _H	003A34 _H	003C34 _H	003E34 _H	ID register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
003635 _H	003835 _H	003A35 _H	003C35 _H	003E35 _H				XXXXXXXX _B XXXXXXXX _B
003636 _H	003836 _H	003A36 _H	003C36 _H	003E36 _H				XXXXXXXX _B XXXXXXXX _B
003637 _H	003837 _H	003A37 _H	003C37 _H	003E37 _H				XXXXXXXX _B XXXXXXXX _B
003638 _H	003838 _H	003A38 _H	003C38 _H	003E38 _H	ID register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
003639 _H	003839 _H	003A39 _H	003C39 _H	003E39 _H				XXXXXXXX _B XXXXXXXX _B
00363A _H	00383A _H	003A3A _H	003C3A _H	003E3A _H				XXXXXXXX _B XXXXXXXX _B
00363B _H	00383B _H	003A3B _H	003C3B _H	003E3B _H				XXXXXXXX _B XXXXXXXX _B
00363C _H	00383C _H	003A3C _H	003C3C _H	003E3C _H	ID register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
00363D _H	00383D _H	003A3D _H	003C3D _H	003E3D _H				XXXXXXXX _B XXXXXXXX _B
00363E _H	00383E _H	003A3E _H	003C3E _H	003E3E _H				XXXXXXXX _B XXXXXXXX _B
00363F _H	00383F _H	003A3F _H	003C3F _H	003E3F _H				XXXXXXXX _B XXXXXXXX _B

MB90390 Series

List of Message Buffers (ID Registers) (2)

Address					Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003640 _H	003840 _H	003A40 _H	003C40 _H	003E40 _H	ID register 8	IDR8	R/W	XXXXXXXX _B
003641 _H	003841 _H	003A41 _H	003C41 _H	003E41 _H				XXXXXXXX _B
003642 _H	003842 _H	003A42 _H	003C42 _H	003E42 _H				XXXXXXXX _B
003643 _H	003843 _H	003A43 _H	003C43 _H	003E43 _H				XXXXXXXX _B
003644 _H	003844 _H	003A44 _H	003C44 _H	003E44 _H	ID register 9	IDR9	R/W	XXXXXXXX _B
003645 _H	003845 _H	003A45 _H	003C45 _H	003E45 _H				XXXXXXXX _B
003646 _H	003846 _H	003A46 _H	003C46 _H	003E46 _H				XXXXXXXX _B
003647 _H	003847 _H	003A47 _H	003C47 _H	003E47 _H				XXXXXXXX _B
003648 _H	003848 _H	003A48 _H	003C48 _H	003E48 _H	ID register 10	IDR10	R/W	XXXXXXXX _B
003649 _H	003849 _H	003A49 _H	003C49 _H	003E49 _H				XXXXXXXX _B
00364A _H	00384A _H	003A4A _H	003C4A _H	003E4A _H				XXXXXXXX _B
00364B _H	00384B _H	003A4B _H	003C4B _H	003E4B _H				XXXXXXXX _B
00364C _H	00384C _H	003A4C _H	003C4C _H	003E4C _H	ID register 11	IDR11	R/W	XXXXXXXX _B
00364D _H	00384D _H	003A4D _H	003C4D _H	003E4D _H				XXXXXXXX _B
00364E _H	00384E _H	003A4E _H	003C4E _H	003E4E _H				XXXXXXXX _B
00364F _H	00384F _H	003A4F _H	003C4F _H	003E4F _H				XXXXXXXX _B
003650 _H	003850 _H	003A50 _H	003C50 _H	003E50 _H	ID register 12	IDR12	R/W	XXXXXXXX _B
003651 _H	003851 _H	003A51 _H	003C51 _H	003E51 _H				XXXXXXXX _B
003652 _H	003852 _H	003A52 _H	003C52 _H	003E52 _H				XXXXXXXX _B
003653 _H	003853 _H	003A53 _H	003C53 _H	003E53 _H				XXXXXXXX _B
003654 _H	003854 _H	003A54 _H	003C54 _H	003E54 _H	ID register 13	IDR13	R/W	XXXXXXXX _B
003655 _H	003855 _H	003A55 _H	003C55 _H	003E55 _H				XXXXXXXX _B
003656 _H	003856 _H	003A56 _H	003C56 _H	003E56 _H				XXXXXXXX _B
003657 _H	003857 _H	003A57 _H	003C57 _H	003E57 _H				XXXXXXXX _B
003658 _H	003858 _H	003A58 _H	003C58 _H	003E58 _H	ID register 14	IDR14	R/W	XXXXXXXX _B
003659 _H	003859 _H	003A59 _H	003C59 _H	003E59 _H				XXXXXXXX _B
00365A _H	00385A _H	003A5A _H	003C5A _H	003E5A _H				XXXXXXXX _B
00365B _H	00385B _H	003A5B _H	003C5B _H	003E5B _H				XXXXXXXX _B
00365C _H	00385C _H	003A5C _H	003C5C _H	003E5C _H	ID register 15	IDR7	R/W	XXXXXXXX _B
00365D _H	00385D _H	003A5D _H	003C5D _H	003E5D _H				XXXXXXXX _B
00365E _H	00385E _H	003A5E _H	003C5E _H	003E5E _H				XXXXXXXX _B
00365F _H	00385F _H	003A5F _H	003C5F _H	003E5F _H				XXXXXXXX _B

List of Message Buffers (DLC Registers and Data Registers) (1)

Address					Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003660 _H	003860 _H	003A60 _H	003C60 _H	003E60 _H	DLC register 0	DLCR0	R/W	XXXXXXXX _B
003661 _H	003861 _H	003A61 _H	003C61 _H	003E61 _H				
003662 _H	003862 _H	003A62 _H	003C62 _H	003E62 _H	DLC register 1	DLCR1	R/W	XXXXXXXX _B
003663 _H	003863 _H	003A63 _H	003C63 _H	003E63 _H				
003664 _H	003864 _H	003A64 _H	003C64 _H	003E64 _H	DLC register 2	DLCR2	R/W	XXXXXXXX _B
003665 _H	003865 _H	003A65 _H	003C65 _H	003E65 _H				
003666 _H	003866 _H	003A66 _H	003C66 _H	003E66 _H	DLC register 3	DLCR3	R/W	XXXXXXXX _B
003667 _H	003867 _H	003A67 _H	003C67 _H	003E67 _H				
003668 _H	003868 _H	003A68 _H	003C68 _H	003E68 _H	DLC register 4	DLCR4	R/W	XXXXXXXX _B
003669 _H	003869 _H	003A69 _H	003C69 _H	003E69 _H				
00366A _H	00386A _H	003A6A _H	003C6A _H	003E6A _H	DLC register 5	DLCR5	R/W	XXXXXXXX _B
00366B _H	00386B _H	003A6B _H	003C6B _H	003E6B _H				
00366C _H	00386C _H	003A6C _H	003C6C _H	003E6C _H	DLC register 6	DLCR6	R/W	XXXXXXXX _B
00366D _H	00386D _H	003A6D _H	003C6D _H	003E6D _H				
00366E _H	00386E _H	003A6E _H	003C6E _H	003E6E _H	DLC register 7	DLCR7	R/W	XXXXXXXX _B
00366F _H	00386F _H	003A6F _H	003C6F _H	003E6F _H				
003670 _H	003870 _H	003A70 _H	003C70 _H	003E70 _H	DLC register 8	DLCR8	R/W	XXXXXXXX _B
003671 _H	003871 _H	003A71 _H	003C71 _H	003E71 _H				
003672 _H	003872 _H	003A72 _H	003C72 _H	003E72 _H	DLC register 9	DLCR9	R/W	XXXXXXXX _B
003673 _H	003873 _H	003A73 _H	003C73 _H	003E73 _H				
003674 _H	003874 _H	003A74 _H	003C74 _H	003E74 _H	DLC register 10	DLCR10	R/W	XXXXXXXX _B
003675 _H	003875 _H	003A75 _H	003C75 _H	003E75 _H				
003676 _H	003876 _H	003A76 _H	003C76 _H	003E76 _H	DLC register 11	DLCR11	R/W	XXXXXXXX _B
003677 _H	003877 _H	003A77 _H	003C77 _H	003E77 _H				
003678 _H	003878 _H	003A78 _H	003C78 _H	003E78 _H	DLC register 12	DLCR12	R/W	XXXXXXXX _B
003679 _H	003879 _H	003A79 _H	003C79 _H	003E79 _H				
00367A _H	00387A _H	003A7A _H	003C7A _H	003E7A _H	DLC register 13	DLCR13	R/W	XXXXXXXX _B
00367B _H	00387B _H	003A7B _H	003C7B _H	003E7B _H				
00367C _H	00387C _H	003A7C _H	003C7C _H	003E7C _H	DLC register 14	DLCR14	R/W	XXXXXXXX _B
00367D _H	00387D _H	003A7D _H	003C7D _H	003E7D _H				
00367E _H	00387E _H	003A7E _H	003C7E _H	003E7E _H	DLC register 15	DLCR15	R/W	XXXXXXXX _B
00367F _H	00387F _H	003A7F _H	003C7F _H	003E7F _H				

MB90390 Series

List of Message Buffers (DLC Registers and Data Registers) (2)

Address					Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
003680 _H to 003687 _H	003880 _H to 003887 _H	003A80 _H to 003A87 _H	003C80 _H to 003C87 _H	003E80 _H to 003E87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
003688 _H to 00368F _H	003888 _H to 00388F _H	003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	003E88 _H to 003E8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003690 _H to 003697 _H	003890 _H to 003897 _H	003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	003E90 _H to 003E97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003698 _H to 00369F _H	003898 _H to 00389F _H	003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	003E98 _H to 003E9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
0036A0 _H to 0036A7 _H	0038A0 _H to 0038A7 _H	003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	003EA0 _H to 003EA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
0036A8 _H to 0036AF _H	0038A8 _H to 0038AF _H	003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	003EA8 _H to 003EAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
0036B0 _H to 0036B7 _H	0038B0 _H to 0038B7 _H	003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	003EB0 _H to 003EB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
0036B8 _H to 0036BF _H	0038B8 _H to 0038BF _H	003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	003EB8 _H to 003EBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
0036C0 _H to 0036C7 _H	0038C0 _H to 0038C7 _H	003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	003EC0 _H to 003EC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
0036C8 _H to 0036CF _H	0038C8 _H to 0038CF _H	003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	003EC8 _H to 003ECF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
0036D0 _H to 0036D7 _H	0038D0 _H to 0038D7 _H	003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	003ED0 _H to 003ED7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
0036D8 _H to 0036DF _H	0038D8 _H to 0038DF _H	003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	003ED8 _H to 003EDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
0036E0 _H to 0036E7 _H	0038E0 _H to 0038E7 _H	003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	003EE0 _H to 003EE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
0036E8 _H to 0036EF _H	0038E8 _H to 0038EF _H	003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	003EE8 _H to 003EEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

List of Message Buffers (DLC Registers and Data Registers) (3)

Address					Register	Abbrevia- tion	Access	Initial Value
CAN0	CAN1	CAN2	CAN3	CAN4				
0036F0 _H to 0036F7 _H	0038F0 _H to 0038F7 _H	003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	003EF0 _H to 003EF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
0036F8 _H to 0036FF _H	0038F8 _H to 0038FF _H	003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	003EF8 _H to 003EFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

MB90390 Series

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC _H	—	—
INT9 instruction	N/A	#09	FFFFD8 _H	—	—
Exception	N/A	#10	FFFFD4 _H	—	—
Time Base Timer	N/A	#11	FFFFD0 _H	ICR00	0000B0 _H
External Interrupt INT0 to INT7	○	#12	FFFFCC _H		
CAN 0 RX	N/A	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 0 TX/NS	N/A	#14	FFFFC4 _H		
CAN 1 RX	N/A	#15	FFFFC0 _H	ICR02	0000B2 _H
CAN 1 TX/NS	N/A	#16	FFFFBC _H		
PPG 0/1 / (CAN 2 RX)	N/A	#17	FFFFB8 _H	ICR03	0000B3 _H
PPG 2/3 / (CAN 2 TX/NS)	N/A	#18	FFFFB4 _H		
PPG 4/5 / (CAN 3 RX)	N/A	#19	FFFFB0 _H	ICR04	0000B4 _H
PPG 6/7 / (CAN 3 TX/NS)	N/A	#20	FFFFAC _H		
PPG 8/9 / (CAN 4 RX)	N/A	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG A/B / (CAN 4 TX/NS)	N/A	#22	FFFFA4 _H		
16-bit Reload Timer 0	○	#23	FFFFA0 _H	ICR06	0000B6 _H
16-bit Reload Timer 1	○	#24	FFFF9C _H		
Input Capture 0/1	○	#25	FFFF98 _H	ICR07	0000B7 _H
Output compare 0/1	○	#26	FFFF94 _H		
Input Capture 2/3 / Output Compare 6	○	#27	FFFF90 _H	ICR08	0000B8 _H
Output Compare 2/3	○	#28	FFFF8C _H		
Input Capture 4/5 / Output Compare 7	○	#29	FFFF88 _H	ICR09	0000B9 _H
Output Compare 4/5 / I ² C	○	#30	FFFF84 _H		
A/D Converter	○	#31	FFFF80 _H	ICR10	0000BA _H
16-bit Free Run Timer 0/1 / Watch Timer	N/A	#32	FFFF7C _H		
Serial I/O	○	#33	FFFF78 _H	ICR11	0000BB _H
Sound Generator	N/A	#34	FFFF74 _H		
UART 0 RX	◎	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 TX	○	#36	FFFF6C _H		
UART 1 RX	◎	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 TX	○	#38	FFFF64 _H		

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Interrupt cause	EI ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
(UART 2 RX) / UART 3 RX	○	#39	FFFF60 _H	ICR14	0000BE _H
(UART 2 TX) / UART 3 TX	○	#40	FFFF5C _H		
Flash Memory	N/A	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N/A	#42	FFFF54 _H		

○ : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

○ : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Note : For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.

At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.

If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

MB90390 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

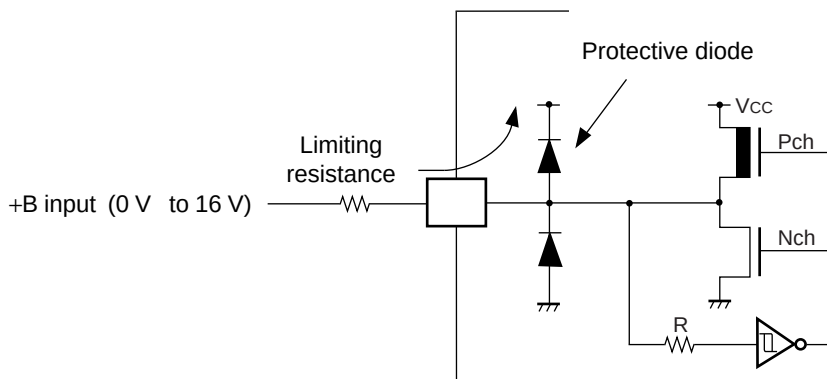
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}^{*2}$
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH, AV_{CC} \geq AVRL, AVRH \geq AVRL$
	DV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} \geq DV_{CC}$
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	*6
Total Maximum Clamp Current	$\Sigma I_{CLAMP} $	—	40	mA	*6
"L" level maximum output current	I_{OL1}	—	15	mA	Normal outputs*4
"L" level average output current	I_{OLAV1}	—	4	mA	Normal outputs, average value
"L" level maximum output current	I_{OL2}	—	40	mA	High current outputs*5
"L" level average output current	I_{OLAV2}	—	30	mA	High current outputs, average value
"L" level maximum overall output current	ΣI_{OL1}	—	100	mA	Sum of all normal outputs
"L" level maximum overall output current	ΣI_{OL2}	—	330	mA	Sum of all high current outputs
"L" level average overall output current	ΣI_{OLAV1}	—	50	mA	Sum of all normal outputs, average value
"L" level average overall output current	ΣI_{OLAV2}	—	250	mA	Sum of all high current outputs, average value
"H" level maximum output current	I_{OH1}	—	-15	mA	Normal outputs*4
"H" level average output current	I_{OHAV1}	—	-4	mA	Normal outputs, average value
"H" level maximum output current	I_{OH2}	—	-40	mA	High current outputs*5
"H" level average output current	I_{OHAV2}	—	-30	mA	High current outputs, average value
"H" level maximum overall output current	ΣI_{OH1}	—	-100	mA	Sum of all normal outputs
"H" level maximum overall output current	ΣI_{OH2}	—	-330	mA	Sum of all high current outputs
"H" level average overall output current	ΣI_{OHAV1}	—	-50	mA	Sum of all normal outputs, average value
"H" level average overall output current	ΣI_{OHAV2}	—	-250	mA	Sum of all high current outputs, average value
Power consumption	P_D	—	800	mW	MB90F394HA/MB90394HA
		—	950	mW	MB90F395HA
Operating temperature	T_A	-40	+85	°C	
Storage temperature	T_{STG}	-55	+150	°C	

(Continued)

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- *1 : The parameter is based on $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$.
- *2 : Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.
- *3 : V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. For ports P70 to P77, P80 to P87 and PA0 to PA7, V_I and V_O should not exceed $DV_{CC} + 0.3\text{ V}$.
- *4 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P90 to P97, PB0 to PB7
- *5 : Applicable to pins : P70 to P77, P80 to P87, PA0 to PA7
- *6 :
 - Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, PB0 to PB7
 - Use within recommended operating conditions.
 - Use at DC voltage (current)
 - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
 - Care must be taken not to leave the +B input pin open.
 - Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
 - Sample recommended circuits:

• Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB90390 Series

2. Recommended Conditions

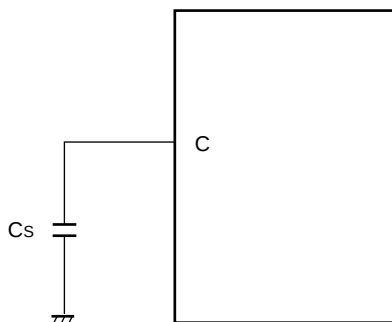
($V_{SS} = AV_{SS} = DV_{SS} = 0\text{ V}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.0	5.5	V	Under normal operation
		4.0	5.0	5.5	V	Under normal operation, when not using the A/D converter
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not programming or erasing Flash
		2.0	—	5.5	V	Retain RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	μF	MB90F394HA/MB90394HA*
		0.22	—	1.0	μF	MB90F395HA*
Operating temperature	T_A	-40	—	+85	$^{\circ}\text{C}$	

* : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the V_{CC} pin (pin 15), use a bypass capacitor that has a larger capacity than that of C_S . On the other V_{CC} pin (pin 105), use a bypass capacitor of about $0.1\text{ }\mu\text{F}$.

Refer to the following figure for connection of smoothing capacitor C_S .

• C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS Hysteresis input levels are selected (except SIN and I ² C pins of MB90394HA/F395HA)
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	MB90394HA/F395HA : SIN (UART, SIO) and I ² C input pins if CMOS Hysteresis levels are selected
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if AUTOMOTIVE Hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input "L" voltage	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS Hysteresis input levels are selected (except SIN and I ² C pins of MB90394HA/F395HA)
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	MB90394HA/F395HA : SIN (UART, SIO) and I ² C input pins if CMOS Hysteresis levels are selected
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if AUTOMOTIVE Hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{RST}$ input pin (CMOS Hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output "H" voltage	V_{OH1}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH1} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	

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MB90390 Series

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$)

Parameter	Sym- bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “H” voltage	V _{OH2}	High current outputs	DV _{CC} = 4.5 V, I _{OH2} = −40.0 mA	DV _{CC} − 0.5	—	—	V	T _A = − 40 °C
			DV _{CC} = 4.5 V, I _{OH2} = −30.0 mA					T _A = + 25 °C
			DV _{CC} = 4.5 V, I _{OH2} = −30.0 mA					T _A = + 85 °C
Output “L” voltage	V _{OL1}	Normal outputs	V _{CC} = 4.5 V, I _{OL1} = 4.0 mA	—	—	0.4	V	
Output “L” voltage	V _{OL2}	High current outputs	DV _{CC} = 4.5 V, I _{OL2} = 40.0 mA	—	—	0.5	V	T _A = − 40 °C
			DV _{CC} = 4.5 V, I _{OL2} = 30.0 mA					T _A = + 25 °C
			DV _{CC} = 4.5 V, I _{OL2} = 30.0 mA					T _A = + 85 °C
Input leak current	I _{IL}	—	V _{CC} = 5.5 V, V _{SS} < V _I < V _{CC}	−5	—	+ 5	μA	
Power supply current*	I _{CC}	V _{CC}	V _{CC} = 5.0 V, Internal frequency : 20 MHz, At normal operation.	—	50	70	mA	MB90394HA/ MB90F394HA
				—	55	75	mA	MB90F395HA
			V _{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	60	85	mA	MB90394HA/ MB90F394HA
				—	65	90	mA	MB90F395HA
			V _{CC} = 5.0 V, Internal frequency : 20 MHz, At writing Flash memory.	—	65	85	mA	MB90F394HA
				—	70	90	mA	MB90F395HA
			V _{CC} = 5.0 V, Internal frequency : 20 MHz, At erasing Flash memory.	—	70	90	mA	MB90F394HA
				—	75	95	mA	MB90F395HA
	I _{CCS}		V _{CC} = 5.0 V, Internal frequency : 24 MHz, At Sleep mode.	—	27	36	mA	MB90394HA/ MB90F394HA
				—	30	40	mA	MB90F395HA

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($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CTS}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency : 2 MHz, At Main Timebase timer mode	—	0.3	0.55	mA	MB90394HA/ MB90F394HA/ MB90F395HA
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At PLL Timebase timer mode, external frequency = 4 MHz	—	5	7	mA	MB90394HA/ MB90F394HA/ MB90F395HA
	I_{CCH}		$V_{CC} = 5.0\text{ V}$, At Stop mode, $T_A = +25^{\circ}\text{C}$	—	5	30	μA	MB90394HA/ MB90F394HA/ MB90F395HA
Input capacitance	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS} , DV_{CC} , DV_{SS} , P70 to P77, P80 to P87, PA0 to PA7	—	—	5	15	pF	
		P70 to P77, P80 to P87, PA0 to PA7	—	—	15	30	pF	

* : The power supply current is measured with an external clock.

4. AC Characteristics

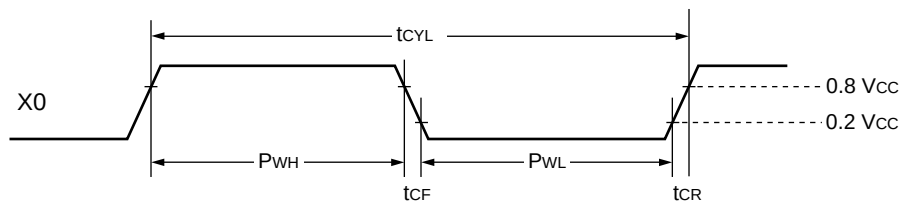
(1) Clock Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$)

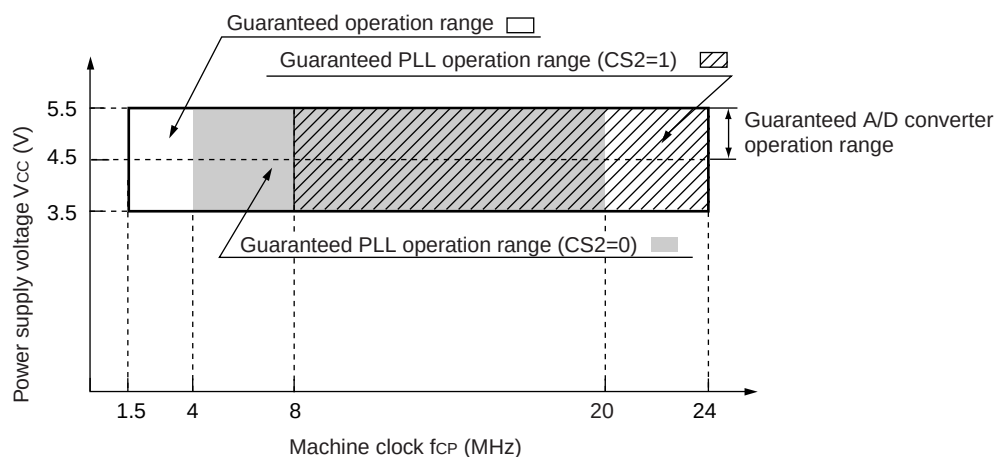
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_c	X0, X1	4	—	8	MHz	When using an oscillator circuit
			4	—	8	MHz	PLL multiplied by 1 When using an oscillator circuit
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit
			4	—	6.67	MHz	PLL multiplied by 3 When using an oscillator circuit (at PSCCR:CS2 = 0)
			4	—	6	MHz	PLL multiplied by 4 When using an oscillator circuit
			4	—	4	MHz	PLL multiplied by 6 When using an oscillator circuit
		X0	3	—	12	MHz	When using an external clock*
Clock cycle time	t_{CYL}	X0, X1	125	—	333	ns	When using a crystal oscillator or a ceramic oscillator
		X0	83.33	—	333	ns	When using an external clock
Input clock pulse width	P_{WH}, P_{WL}	X0	20	—	—	ns	Duty ratio is about 30% to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	24	MHz	Except programming or erasing Flash memory. When using clock modulation, be sure that the maximum momentary fre- quency F_{max} does not exceed 24 MHz. Refer to the Clock Modulator chapter of the Hardware Manual.
		—	1.5	—	20	MHz	When programming or erasing Flash memory. Be sure that the maximum momentary frequency F_{max} does not exceed 20 MHz.
Machine clock cycle time	t_{CP}	—	41.67	—	666	ns	Except programming or erasing Flash memory.
		—	50	—	666	ns	When programming or erasing Flash memory.

* : When using the PLL, there are limits on the range of clock frequencies. Use the PLL within the range shown in the graph in "Guaranteed PLL operation range - The relationship between the external clock frequency and machine clock frequency".

- Clock Timing

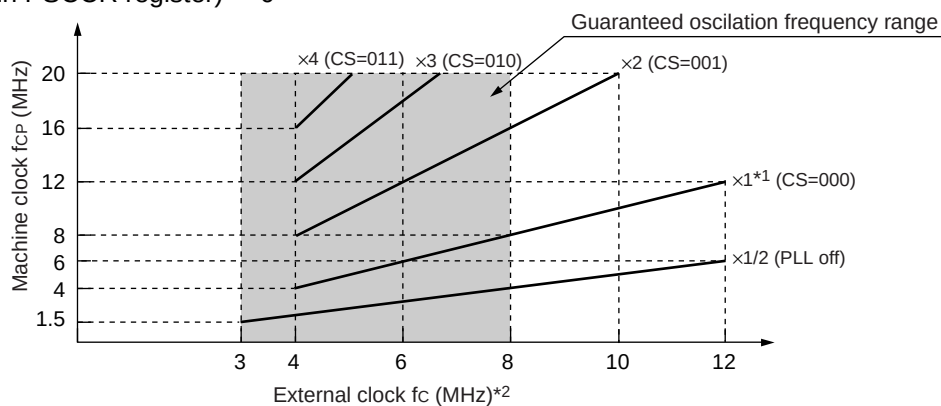


- Guaranteed PLL operation range

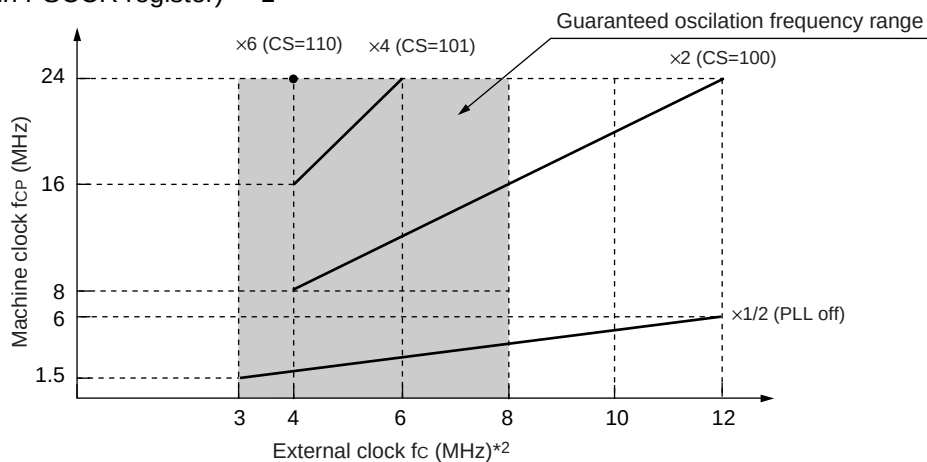


Guaranteed operation range of MB90394HA/MB90F394HA/MB90F395HA

- CS2 (bit 0 in PSCCR register) = 0



- CS2 (bit 0 in PSCCR register) = 1



*1 : PLL $\times 1$ guaranteed operation range is from 4.0 MHz to 12 MHz.

*2 : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 8 MHz

External clock frequency and Machine clock frequency

(2) Reset Standby Input

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	$16\ t_{CP}^{*1}$	—	ns	Under normal operation
			Oscillation time of oscillator ^{*2} + $100\ \mu\text{s}$ + $16\ t_{CP}^{*1}$	—	ns	In Stop mode
			100	—	μs	In Time Base Timer mode

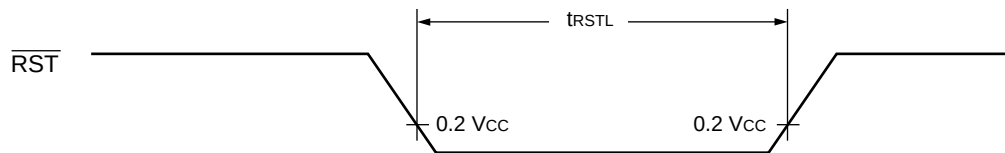
*1 : t_{CP} is the machine clock cycle time. Refer to “(1) Clock timing”.

No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

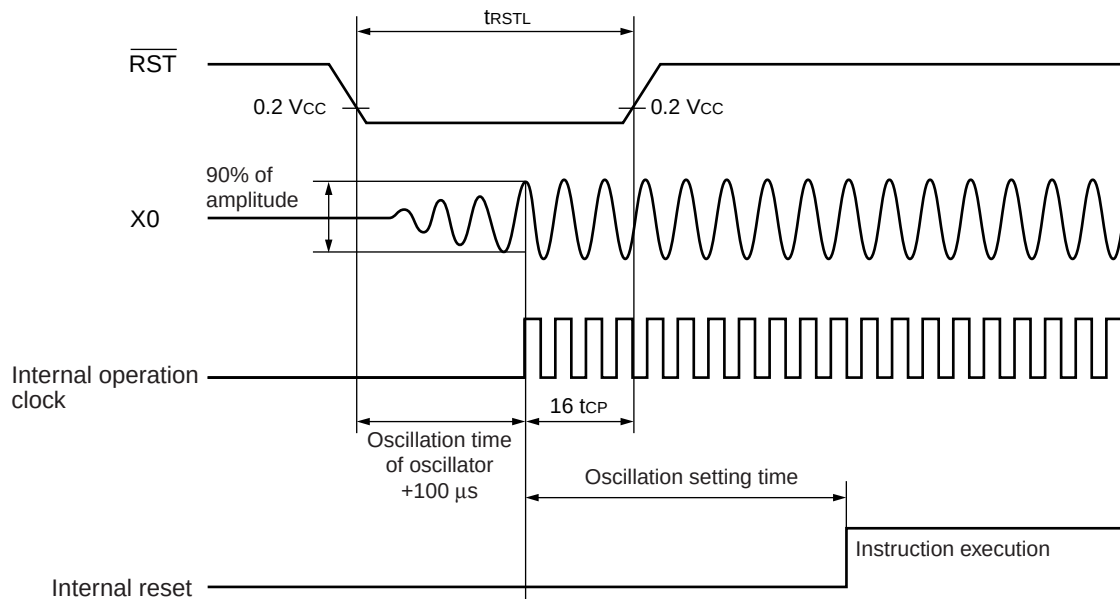
*2 : Oscillation time of oscillator is the time that the amplitude reaches 90%.

In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs to several ms. With an external clock, the oscillation time is 0 ms.

• Under Normal Operation



• In Stop Mode

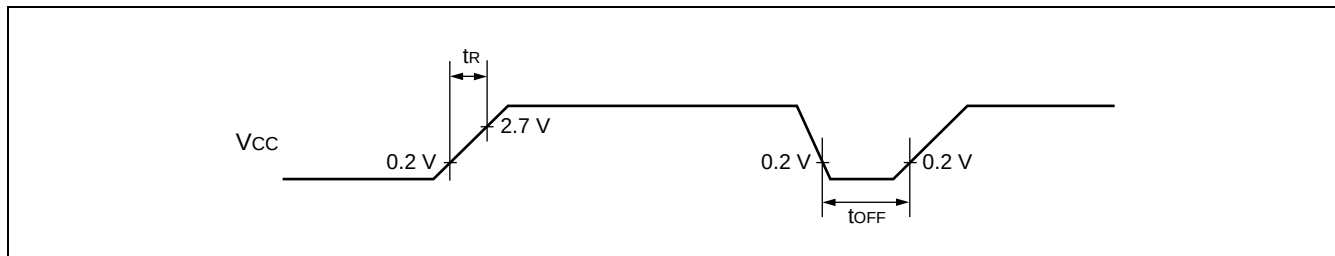


MB90390 Series

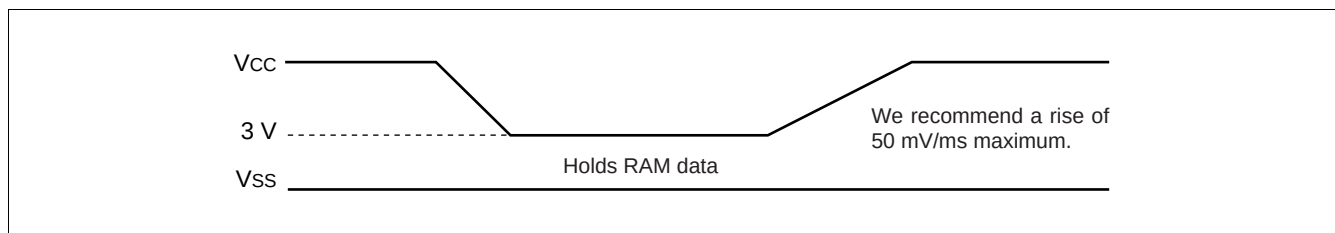
(3) Power On Reset

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = AV_{SS} = DV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Wait time until power on



Note : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you start up smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



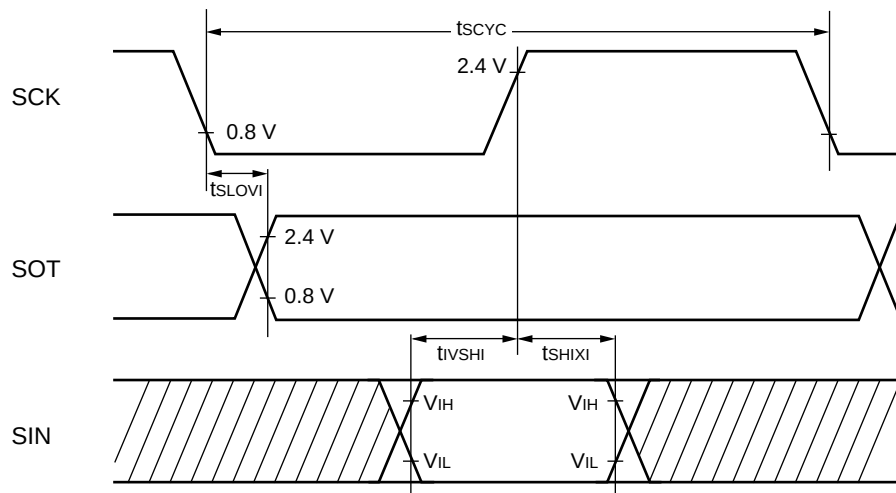
(4) UART0/1 and Serial I/O Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

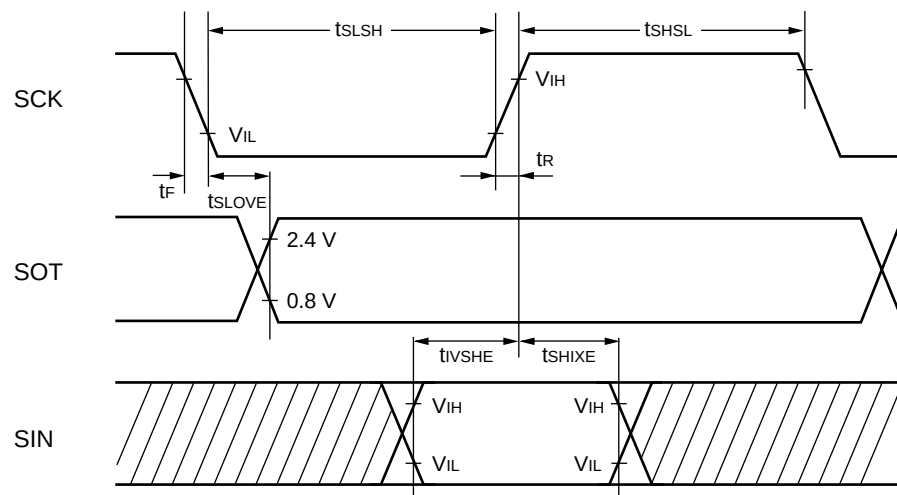
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1, SCK4	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$8\text{ }t_{CP}$	—	ns	
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0, SCK1, SCK4, SOT0, SOT1, SOT4		-80	+80	ns	
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		100	—	ns	
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0, SCK1, SCK4	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$4\text{ }t_{CP}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0, SCK1, SCK4		$4\text{ }t_{CP}$	—	ns	
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCK0, SCK1, SCK4, SOT0, SOT1, SOT4		—	150	ns	
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHE}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SCK4, SIN0, SIN1, SIN4		60	—	ns	

- Notes :
- Above rating is the case of CLK synchronized mode.
 - C_L is load capacity value of pins when testing.
 - t_{CP} is the machine clock cycle time. Refer to " (1) Clock timing".

• Internal Shift Clock Mode



- External Shift Clock Mode



(5) UART2/3 (LIN/SCI)

- Bit setting : ESCR2/3 : SCES = 0, ECCR2/3 : SCDE = 0

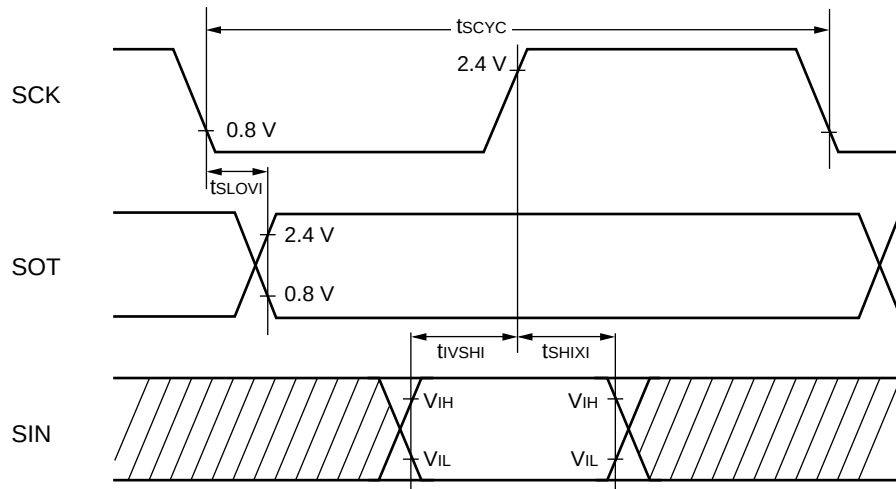
($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2/3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5\text{ }t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK2/3, SOT2/3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCK2/3, SIN2/3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK2/3, SIN2/3		0	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK2/3	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3\text{ }t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK2/3		$t_{CP} + 10$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCK2/3, SOT2/3		—	$2\text{ }t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHE}	SCK2/3, SIN2/3		30	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCK2/3, SIN2/3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK2/3		—	10	ns
SCK rise time	t_R	SCK2/3		—	10	ns

Notes : • C_L is load capacity value of pins when testing.

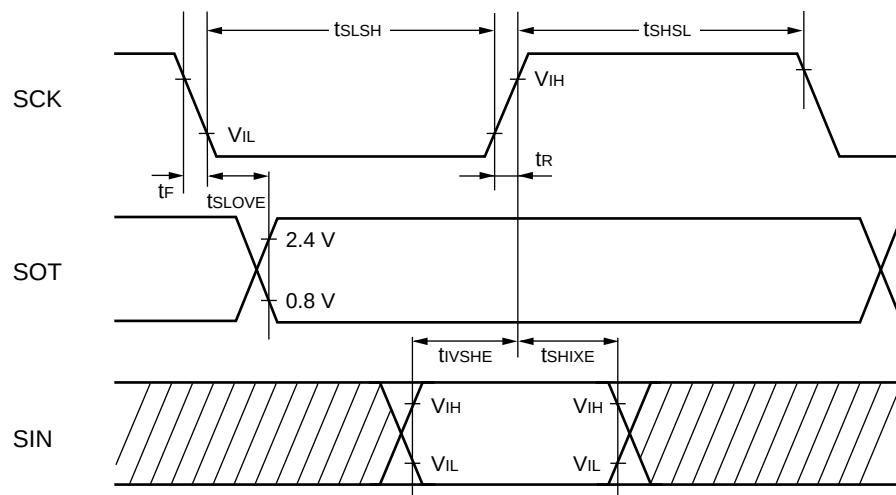
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB90390 series hardware manual".
- t_{CP} is the machine clock cycle time. Refer to " (1) Clock timing".

• Internal Shift Clock Mode



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• External Shift Clock Mode



• Bit setting : ESCR2/3 : SCES = 1, ECCR2/3 : SCDE = 0

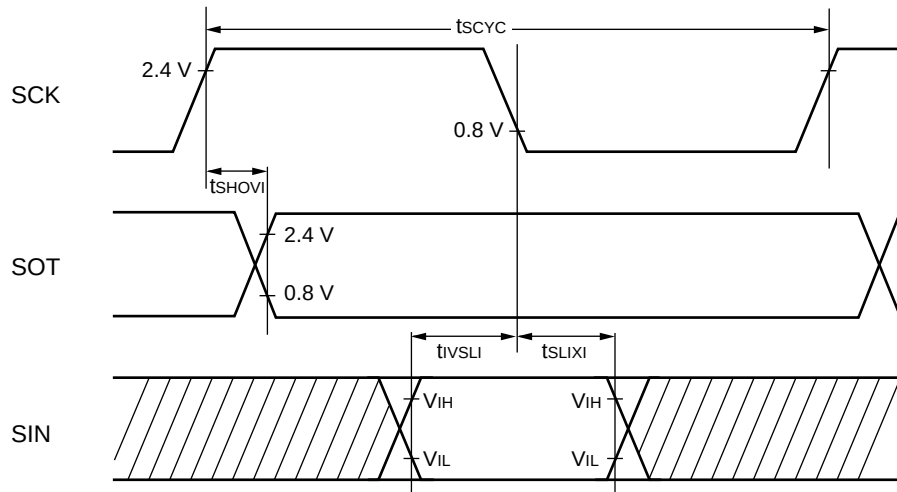
($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK2/3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$5\text{ }t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK2/3, SOT2/3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLI}	SCK2/3, SIN2/3		$t_{CP}+80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCK2/3, SIN2/3		0	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK2/3	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$3\text{ }t_{CP}-t_R$	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK2/3		$t_{CP}+10$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVE}	SCK2/3, SOT2/3		—	$2\text{ }t_{CP}+60$	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLE}	SCK2/3, SIN2/3		30	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXE}	SCK2/3, SIN2/3		$t_{CP}+30$	—	ns
SCK fall time	t_F	SCK2/3		—	10	ns
SCK rise time	t_R	SCK2/3		—	10	ns

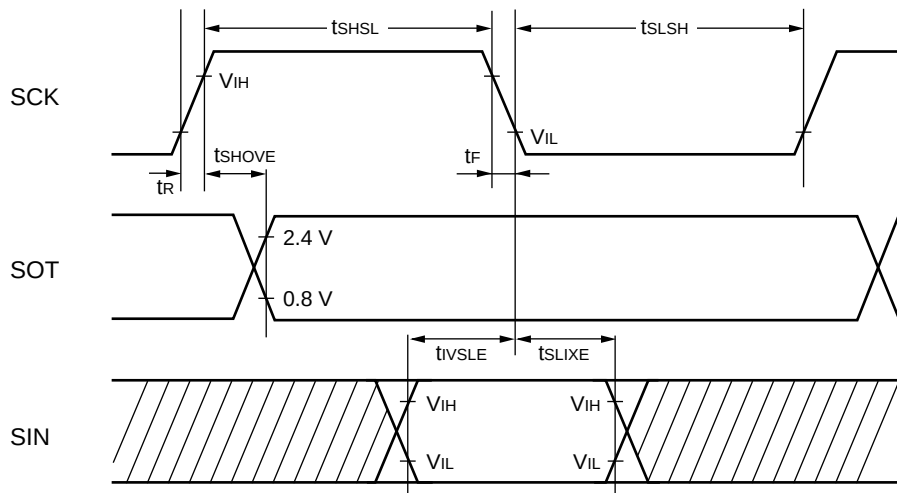
Notes : • C_L is load capacity value of pins when testing.

- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB90390 series hardware manual".
- t_{CP} is the machine clock cycle time. Refer to " (1) Clock timing".

• Internal Shift Clock Mode



• External Shift Clock Mode



MB90390 Series

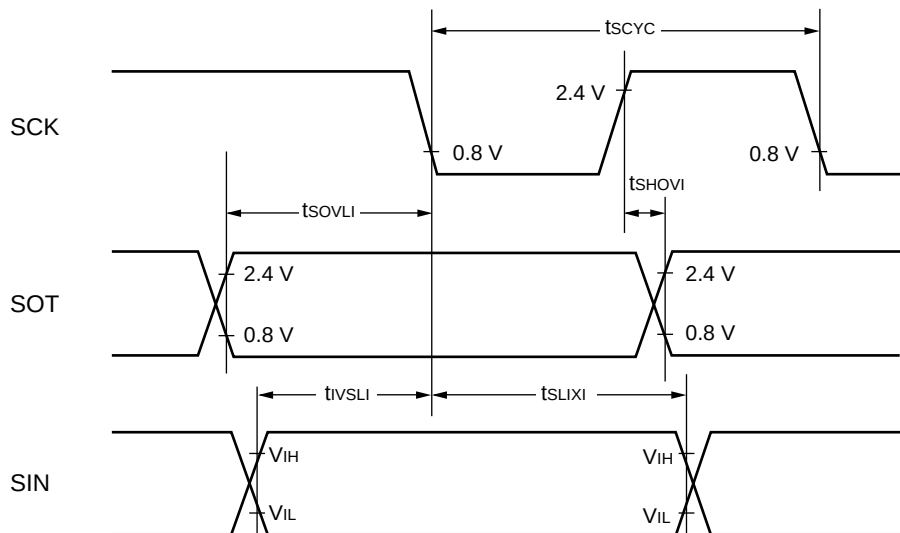
- Bit setting : ESCR2/3 : SCES = 0, ECCR2/3 : SCDE = 1

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Sym- bol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK2/3	Internal clock operation output pins are C _L = 80 pF + 1 TTL	5 t _{CP}	—	ns	
SCK ↑ → SOT delay time	t _{SHOVI}	SCK2/3, SOT2/3		−50	+50	ns	MB90394HA, MB90F395HA, MB90V390HB
				t _{CP} − 60	t _{SCYC} /2 + 70 − t _{CP}	ns	MB90F394HA
Valid SIN → SCK↓	t _{IVSLI}	SCK2/3, SIN2/3		t _{CP} + 80	—	ns	MB90394HA, MB90F395HA, MB90V390HB
				100 − t _{CP}	—	ns	MB90F394HA
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK2/3, SIN2/3		0	—	ns	MB90394HA, MB90F395HA, MB90V390HB
				t _{SCYC} /2	—	ns	MB90F394HA
SOT → SCK ↓ delay time	t _{SOVLI}	SCK2/3, SOT2/3		3 t _{CP} − 70	—	ns	MB90394HA, MB90F395HA, MB90V390HB
			t _{CP} − 60	—	ns	MB90F394HA	

Notes : • C_L is load capacity value of pins when testing.

- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
- t_{CP} is the machine clock cycle time. Refer to “(1) Clock timing”.



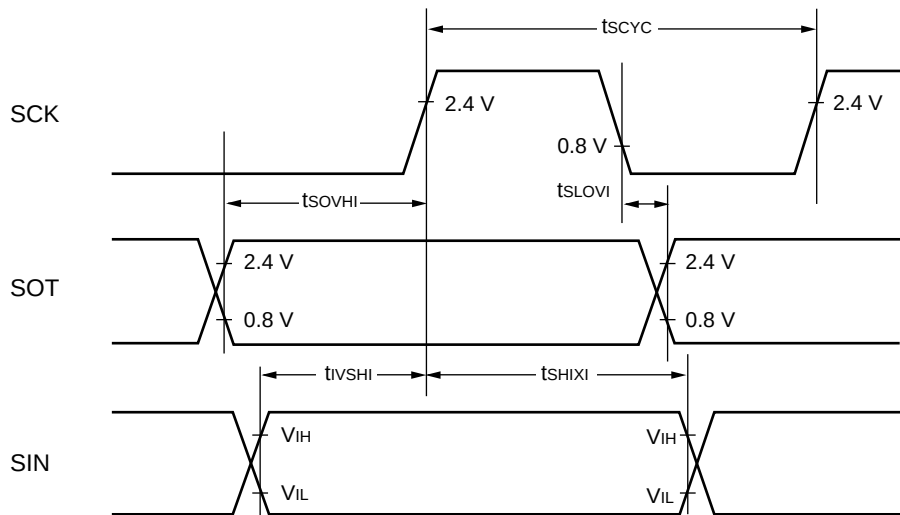
- Bit setting : ESCR2/3 : SCES = 1, ECCR2/3 : SCDE = 1

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Sym- bol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK2/3	Internal clock operation output pins are C _L = 80 pF + 1 TTL	5 t _{CP}	—	ns	
SCK ↓ → SOT delay time	t _{SLOVI}	SCK2/3, SOT2/3		−50	+50	ns	MB90394HA, MB90F395HA, MB90V390HB
				t _{CP} − 60	t _{SCYC} /2 + 70 − t _{CP}	ns	MB90F394HA
Valid SIN → SCK↓	t _{IVSHI}	SCK2/3, SIN2/3		t _{CP} + 80	—	ns	MB90394HA, MB90F395HA, MB90V390HB
				100 − t _{CP}	—	ns	MB90F394HA
SCK ↑ → Valid SIN hold time	t _{SHIXI}	SCK2/3, SIN2/3		0	—	ns	MB90394HA, MB90F395HA, MB90V390HB
				t _{SCYC} /2	—	ns	MB90F394HA
SOT → SCK ↑ delay time	t _{SOVHI}	SCK2/3, SOT2/3		3t _{CP} − 70	—	ns	MB90394HA, MB90F395HA, MB90V390HB
				t _{CP} − 60	—	ns	MB90F394HA

Notes : • C_L is load capacity value of pins when testing.

- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB90390 series hardware manual”.
- t_{CP} is the machine clock cycle time. Refer to “(1) Clock timing”.



MB90390 Series

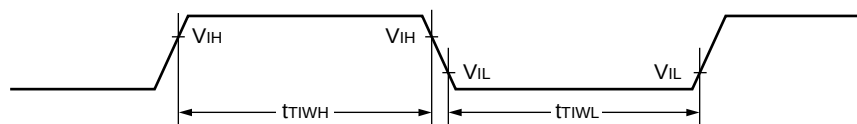
(6) Timer Related Resource Input Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	$4 t_{CP}$	—	ns	
	t_{TIWL}	IN0 to IN5					

Note : t_{CP} is the machine clock cycle time. Refer to “(1) Clock timing”.

• Timer Input Timing



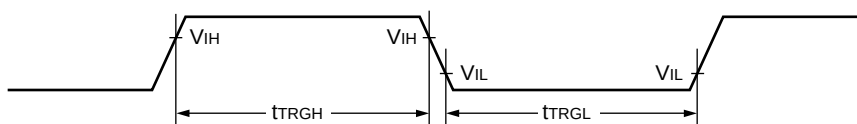
(7) Trigger Input Timing

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	INT0 to INT7	—	200	—	ns	
	t_{TRGL}	ADTG	—	$t_{CP} + 200$	—	ns	

Note : t_{CP} is the machine clock cycle time. Refer to “(1) Clock timing”.

• Trigger Input Timing

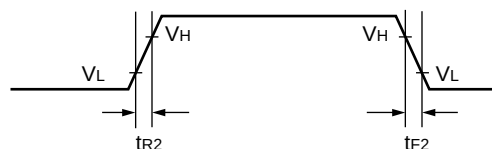


(8) Slew Rate High Current Outputs

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{CC} = DV_{CC} = 3.5\text{ V}$ to 5.5 V , $V_{SS} = DV_{SS} = 0\text{ V}$)

Parameter	Sym- bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{r2} t_{f2}	P70 to P77, P80 to P87, PA0 to PA7	—	15	—	—	ns	

• Slew Rate Output Timing



$$V_H = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$$

$$V_L = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$$

(9) I²C Timing

(T_A = -40 °C to +85 °C, V_{CC} = 3.5 V to 5.5 V, V_{SS} = 0 V)

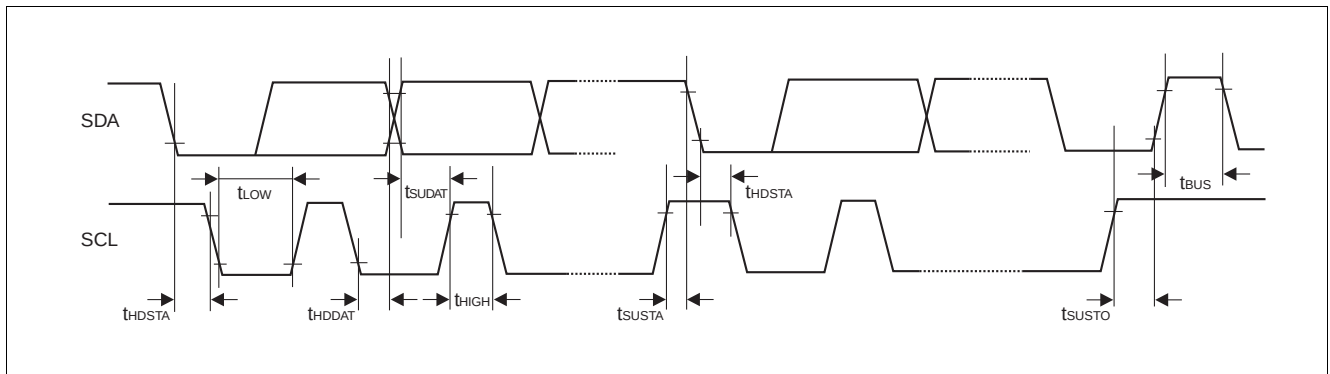
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.3 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs
"L" width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs
"H" width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45*2	0	0.9*3	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t _{BUS}		4.7	—	1.3	—	μs

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} only has to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



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5. A/D Converter

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = \text{AV}_{SS} = 0\text{ V}$)

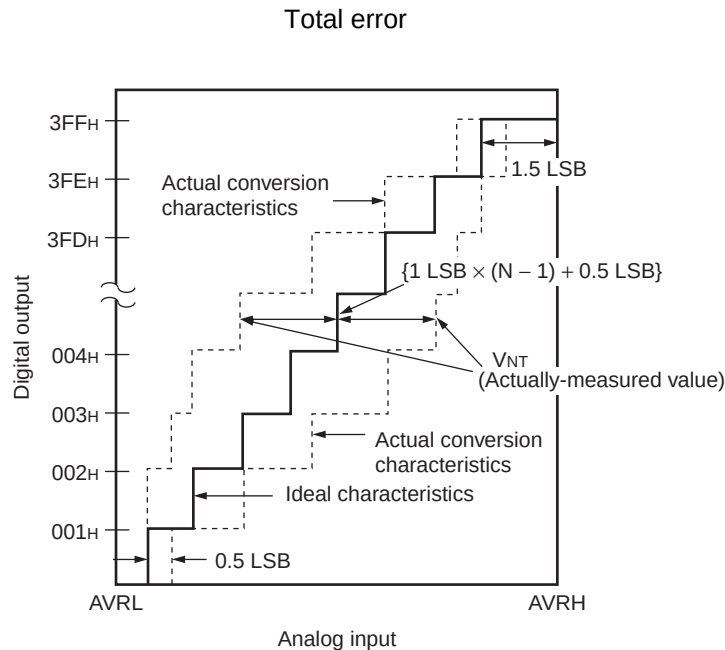
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	± 3.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	$\text{AVRL} - 1.5\text{ LSB}$	$\text{AVRL} + 0.5\text{ LSB}$	$\text{AVRL} + 2.5\text{ LSB}$	V	
Full scale reading voltage	V_{FST}	AN0 to AN14	$\text{AVRH} - 3.5\text{ LSB}$	$\text{AVRH} - 1.5\text{ LSB}$	$\text{AVRH} + 0.5\text{ LSB}$	V	
Compare time	—	—	3.3	—	16500	μs	
			—	$3.3 (= 66\text{ }t_{CP})$	—	μs	$f_{CP} = 20\text{ MHz}$
			—	$3.7 (= 88\text{ }t_{CP})$	—	μs	$f_{CP} = 24\text{ MHz}$
Sampling time	—	—	1.6	—	∞	μs	
			—	$1.6 (= 32\text{ }t_{CP})$	—	μs	$f_{CP} = 20\text{ MHz}$
			—	$2 (= 48\text{ }t_{CP})$	—	μs	$f_{CP} = 24\text{ MHz}$
Analog port input current	I_{AIN}	AN0 to AN14	-1	—	+1	μA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	AV_{CC}	V	
	—	AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AVRH	—	165	250	μA	
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

* : When not operating A/D converter, this is the current ($V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$) .

- Notes :
- The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.
 - t_{CP} is the machine clock cycle time. Refer to “(1) Clock timing” in “4. AC Characteristics”.

6. Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linear error : Deviation between a line across zero-transition line (“00 0000 0000” $\leftarrow \rightarrow$ “00 0000 0001”) and full-scale transition line (“11 1111 1110” $\leftarrow \rightarrow$ “11 1111 1111”) and actual conversion characteristics.
- Differential linear error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

N : A/D converter digital output value

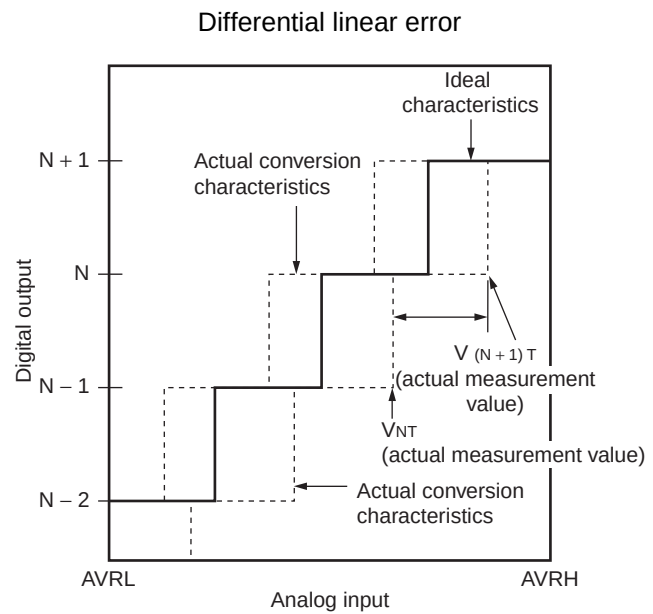
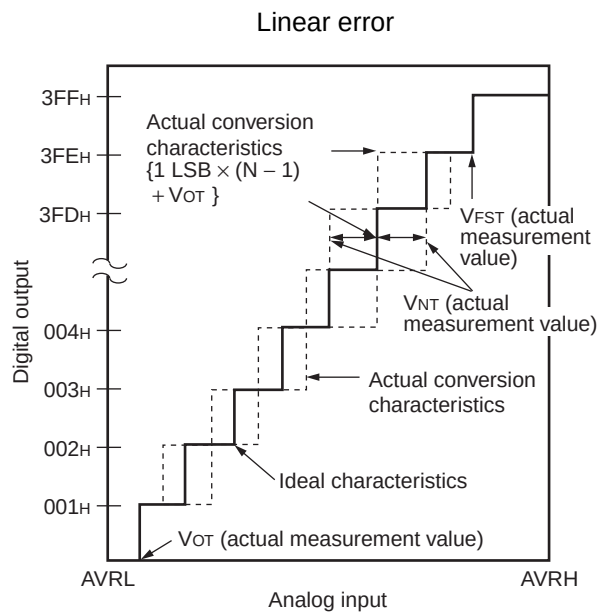
$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB [V]}$$

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

(Continued)

(Continued)



$$\text{Linear error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB} \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

N : A/D converter digital output value

V_{OT} : Voltage at which digital output transits from "000_H" to "001_H".

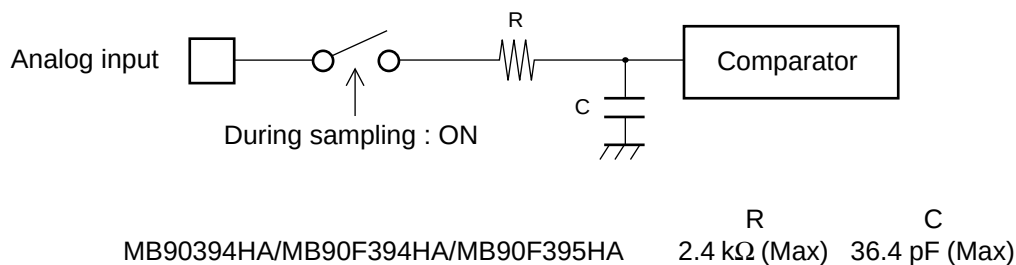
V_{FST} : Voltage at which digital output transits from "3FE_H" to "3FF_H".

7. Notes on A/D Converter Section

- **About the external impedance of the analog input and its sampling time**

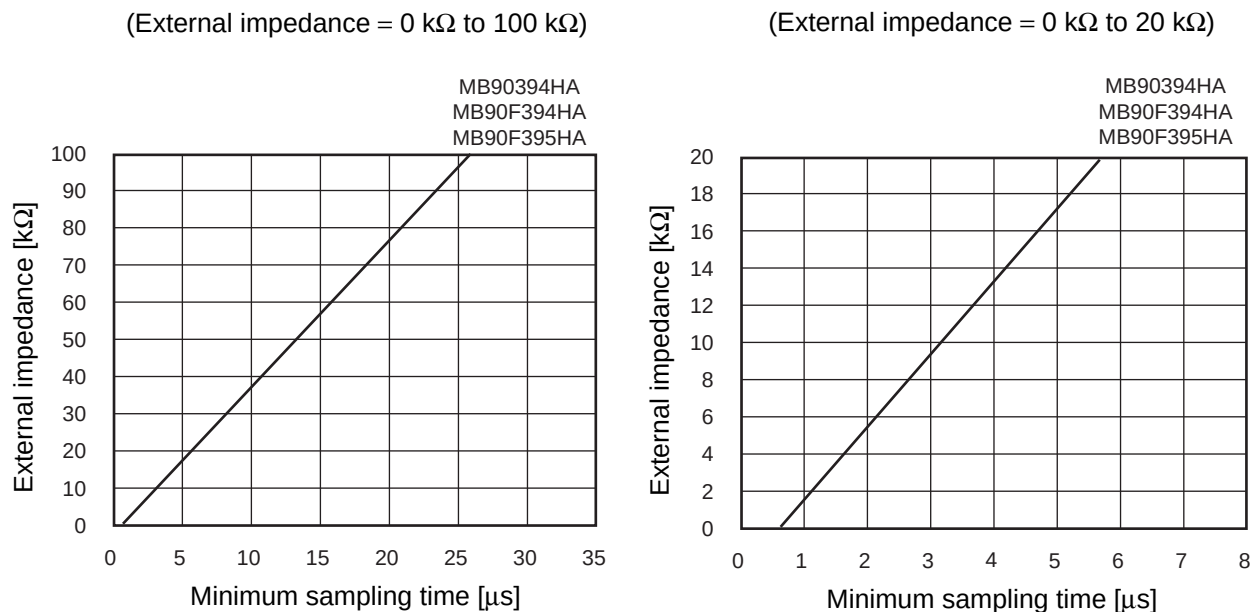
A/D converter with sample & hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample & hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

- Analog input circuit model



Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time



- About the error

The accuracy gets worse as $|AVRH - AVRL|$ becomes smaller.

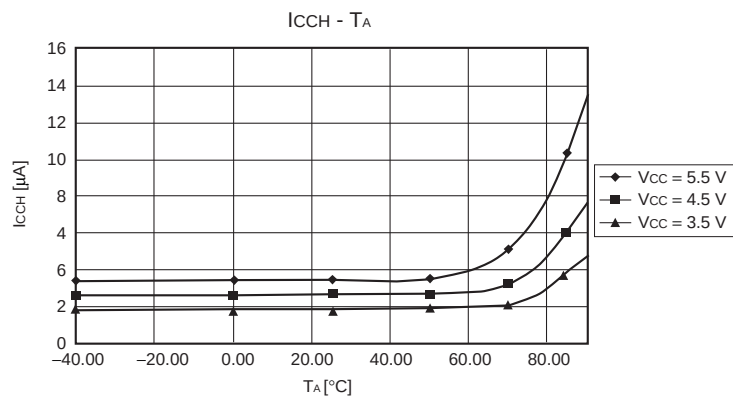
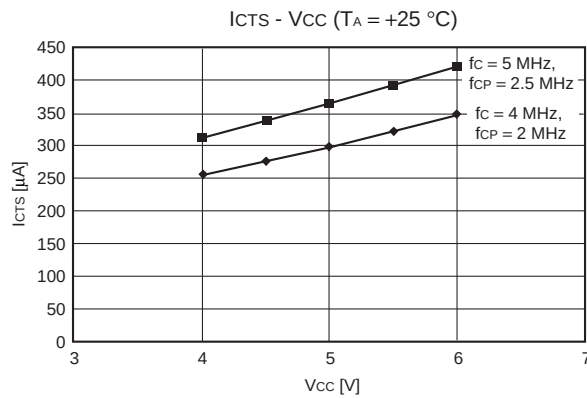
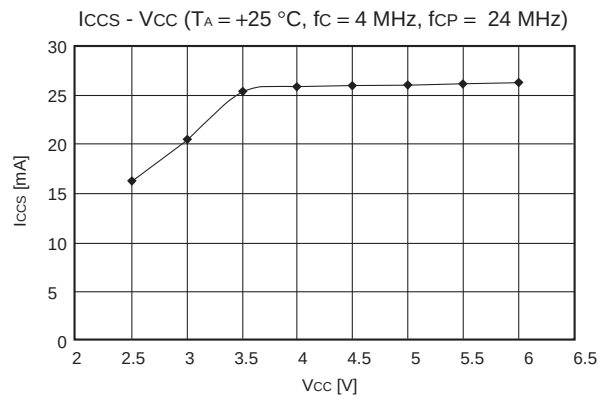
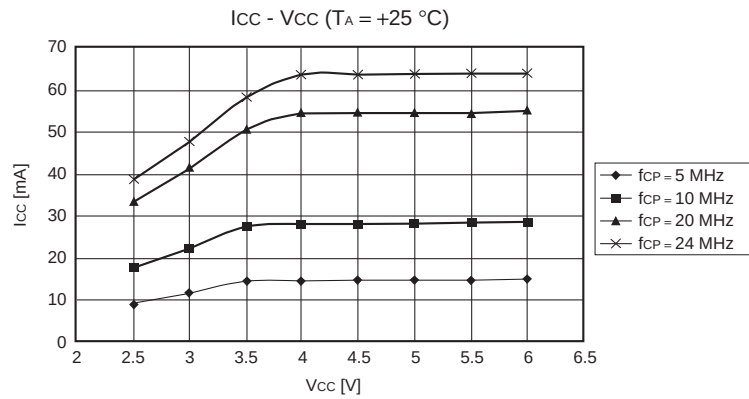
MB90390 Series

8. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T _A = +25 °C V _{CC} = 5.0 V	—	1	15	s	Excludes 00 _H program- ming prior to erasure.
Chip erase time		—	9	—	s	MB90F394HA, Excludes 00 _H programming prior to erasure.
		—	14	—	s	MB90F395HA, Excludes 00 _H programming prior to erasure.
Word (16-bit width) programming time		—	16	3600	μs	Except for the over head time of the system.
Programs/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average T _A = +85 °C	20	—	—	year	*

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

EXAMPLE CHARACTERISTICS

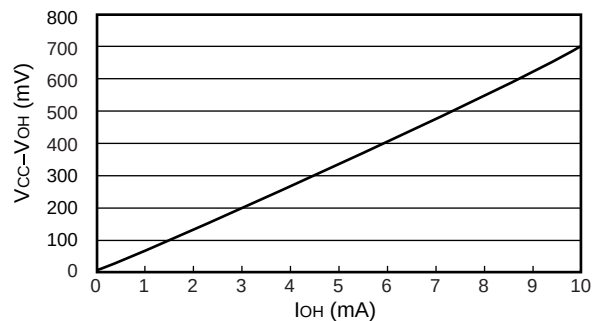


MB90390 Series

• I/O characteristics

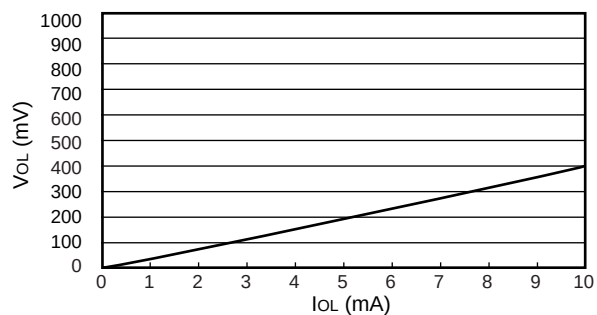
$$(V_{CC} - V_{OH}) - I_{OH}$$

$T_A = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 4.5\text{ V}$



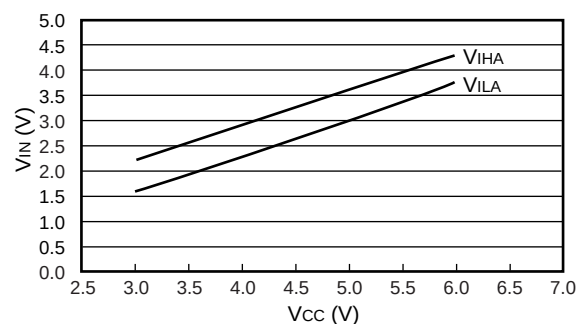
$$V_{OL} - I_{OL}$$

$T_A = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 4.5\text{ V}$



$$\text{Automotive } V_{IN} - V_{CC}$$

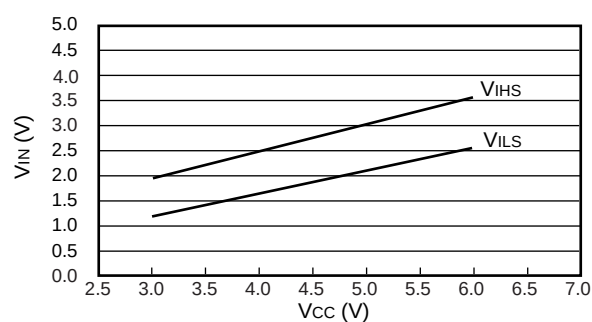
$T_A = +25\text{ }^{\circ}\text{C}$



$$\text{CMOS } V_{IN} - V_{CC}$$

Except UART-SIN pins and
I²C pins of MB90394HA/MB90F395HA

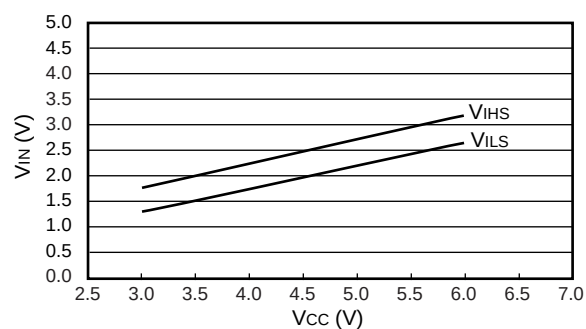
$T_A = +25\text{ }^{\circ}\text{C}$



$$\text{CMOS } V_{IN} - V_{CC}$$

UART-SIN pins and I²C pins of MB90394HA/MB90F395HA

$T_A = +25\text{ }^{\circ}\text{C}$

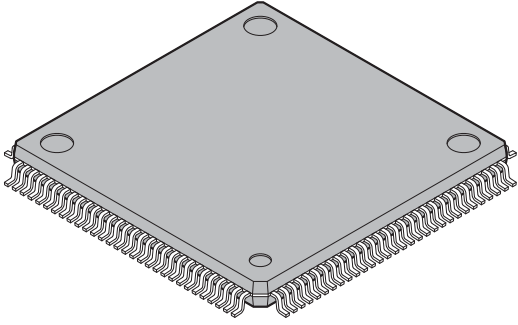


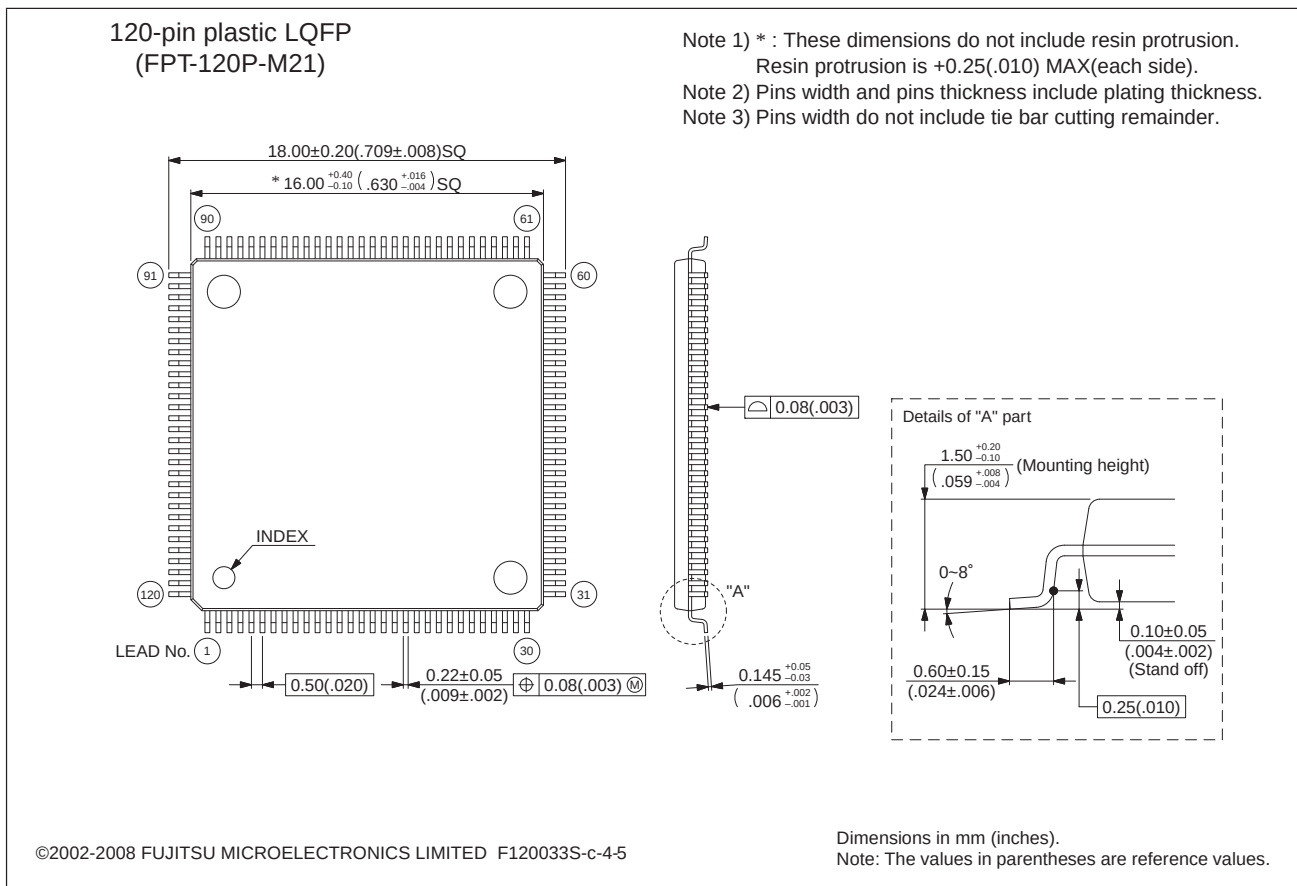
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F394HAPMT	120-pin Plastic LQFP (FPT-120P-M21)	
MB90394HAPMT	120-pin Plastic LQFP (FPT-120P-M21)	
MB90F395HAPMT	120-pin Plastic LQFP (FPT-120P-M21)	
MB90V390HBCR	299-pin Ceramic PGA (PGA-299C-A01)	For evaluation

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■ PACKAGE DIMENSION

 120-pin plastic LQFP (FPT-120P-M21)	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/package/en-search/>

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Added the part number. MB90F395HA
1 to 3	■ DESCRIPTION ■ FEATURES ■ PRODUCT LINEUP	Changed the value of Minimum instruction execution time. 42 ns → 41.7 ns
48	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing	Item: Detailed the clock frequency rated values for each PLL multiplier Added the footnote*.

The vertical lines marked in the left side of the page show the changes.

MB90390 Series

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3329
<http://jp.fujitsu.com/fml/en/>

For further information please contact:

North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
<http://www.fma.fujitsu.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
<http://www.fmal.fujitsu.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
<http://emea.fujitsu.com/microelectronics/>

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
<http://cn.fujitsu.com/fmc/>

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
<http://kr.fujitsu.com/fmk/>

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
<http://cn.fujitsu.com/fmc/en/>

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