AZ DISPLAYS, INC.

SPECIFICATIONS FOR

LIQUID CRYSTAL DISPLAY

PART NUMBER:	AGM2416B
DATE:	September 13, 2005

1 General Specifications

Item	Standard Value	Unit
Display Pattern	☑Dot-Graphic ☐Character ☐Digits ☐_____ ☐with ICON	Dots
Color	☐Mono. ☐Grayscale ☑ FSTN	
Module Dimension	92.0 X 71.8 X 2.0	mm
Viewing Area	67.0 X 46.8	mm
Active Area	62.38 X 42.38	mm
Character Size	/	mm
Character Pitch	/	mm
DOT Size	0.245 X 0.24	mm
DOT Pitch	0.265 X 0.26	mm
LCD Type	☐TN, Positive ☐TN, Negative ☐HTN, Positive ☐HTN, Negative ☐STN, Yellow-Green ☐STN, Gray ☐STN, Blue ☑FSTN, Positive ☐FSTN, Negative ☐Color STN ☐FM LCD	
Polarizer Type	☑Transflective ☐Transmissive ☐Reflective ☐Anti-Glare	
View Direction	☑6H ☐12H ☐_____	
LCD Controller & Driver	ST8016 & ST8024	
LCD Driving Method	1/160duty, 1/14bias	
Interface Type	☐I^2C ☐4-wire Serial ☐3-wire Serial ☐6800 ☐8080 ☑4-bit ☐_____	
Backlight Type	/	
Backlight Color	/	
EL/CCFL Driver type	/	
DC-DC Converter	☐Build-in ☑External	
Operation Temperature (^oC)	-10 ~ 60 (T_{OPL} – T_{OPH})	°C
Storage Temperature (^oC)	-20 ~ 70 (T_{STL} -- T_{STH})	° C

3.1 Pin Description

Segment Pin

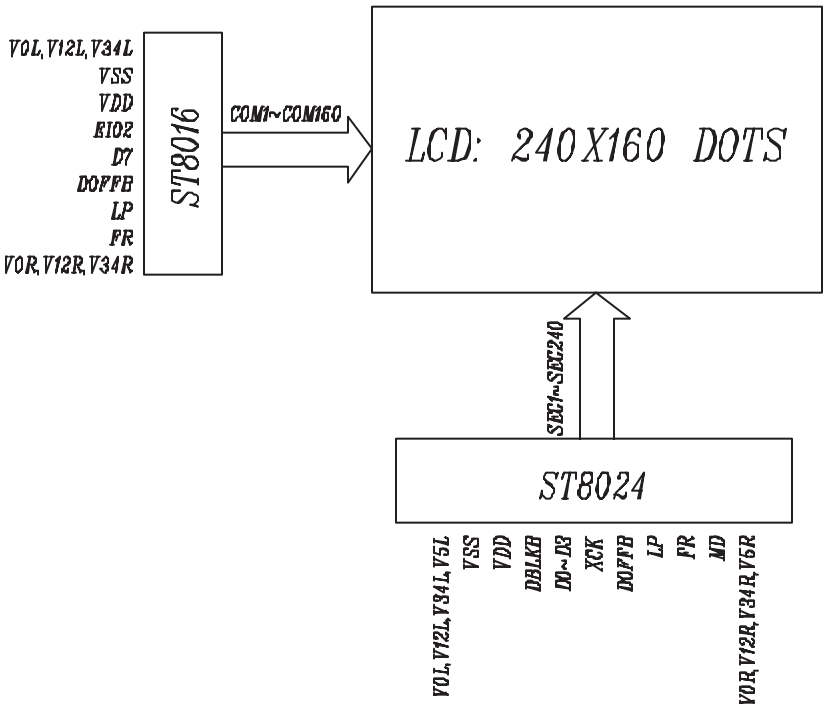
Pin No.	Symbol	Function Description
1	V0L	Bias power supply pins for LCD drive voltage Normally use the bias voltages set by a resistor divider Ensure that voltages are set such that V_{SS} • • $V_5 < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} (i = 0,12, 43, 5) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
2	V12L	
3	V34L	
4	V5L	
5	VSS	Ground
6	VSS	
7	VDD	Logic power supply
8	VDD	
9	DBLKB	Use as contrast control, use PWM signal as input. Connect to V_{DD} for no contrast control.
10	D0	Data bus
11	D1	
12	D2	
13	D3	
14	XCK	Clock input pin for taking display data * Data is read at the falling edge of the clock pulse.
15	DOFFB	Control input pin for output of non-select level The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level Vss. When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of DISPOFF. When the DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
16	LP	Latch pulse input pin for display data Data is latched at the falling edge of the clock pulse.
17	FR	AC signal input pin for LCD drive waveform The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
18	MD	Mode selection pin When set to V_{SS} level "L", 8-bit parallel input mode is set. When set to V_{DD} level "H", 4-bit parallel input mode is set. Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
19	V5R	Bias power supply pins for LCD drive voltage

20	V34R	Normally use the bias voltages set by a resistor divider Ensure that voltages are set such that V_{SS} • • $V_5 < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} (i = 0,12, 43, 5) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
21	V12R	
22	V0R	

Common Pin

Pin No.	Symbol	Function Description
23	V0L	Bias power supply pins for LCD drive voltage Normally use the bias voltages set by a resistor divider. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.
24	V12L	
25	V34L	
26	VSS	Ground
27	VSS	
28	VSS	
29	VDD	Logic power supply
30	VDD	
31	VDD	
32	EIO2	Shift data input for shift register at common mode
33	D7	Dual mode data input at common mode
34	DOFFB	Control input pin for output of non-select level The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level Vss. When set to "L¡±, the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
35	LP	Shift clock pulse input pin for bi-directional shift register * Data is shifted at the falling edge of the clock pulse.
36	FR	AC signal input pin for LCD drive waveform The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
37	V34R	Bias power supply pins for LCD drive voltage Normally use the bias voltages set by a resistor divider. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.
38	V12R	
39	V0R	

3.2 Block Diagram



4. Electrical-optical Specifications

4.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_o	V_{OL}, V_{OR}	-0.3 to +45.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to V_0 + 0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to V_0 + 0.3	V	
	V_5	V_{SL}, V_{SR}	-0.3 toV_0+0.3	V	
Input voltage	V_I	D17-DI0, XCK, LP, L/R, FR, MD, S/C, $\overline{EIO_1}$, EI02, $\overline{DISPOFF}$, $TEST_1$	-0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

4.2 Electrical-Optical Characteristics

No	Item		Symbol	Condition	Min.	Typ.	Max.	Unit
1	Current (all SEG on)		I	Ta=25°C	-	15.0	30.0	mA
2	Contrast Ratio		Cr	Ta=25°C V_{LCD} = 19.5V	4.5	5.0	-	-
3	Threshold voltage		Vth	Ta=25°C	1.85	1.90	-	V
4	Saturation voltage		Vsat	Ta=25°C	-	2.05	2.10	V
5	Response time	Rise time	Tr	Ta=25°C	-	250	350	ms
		Fall time	Tf	Ta=25°C	-	200	300	ms
		On time	T_{ON}	Ta=25°C	-	300	450	ms
6		Off time	T_{OFF}	Ta=25°C	-	250	350	ms
7	Viewing Angle	6H	φ1	Cr = 2 Ta=25°C	45	-	-	Deg.
8		12H	φ2		25	-	-	Deg.
9		3H	φ3		45	-	-	Deg.
10		9H	φ4		45	-	-	Deg.
11	Frame frequency		fM	Ta=25°C	32	64	128	Hz

4.3 Electrical Characteristics

No	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Supply Voltage for Logic	V_{DD}-V_{SS}	-	2.5	-	5.5	V
2	Supply Voltage for LCD Driver	V_{DD}-V_O (V_{LCD})	Ta=25 °C	19.3	19.5	19.7	V
3	Supply Current for Logic	I_{DD}	Ta=25 °C V_{DD}=5.0V	-	23	26	mA
4	Frame Frequency	f_M	Ta=25°C	-	80	-	Hz

5	Input High Voltage	V_{IH}	-	$0.8XV_{DD}$	-	V_{DD}	V
6	Input Low Voltage	V_{IL}	-	GND	-	$0.2XV_{DD}$	V
7	Output High Voltage	V_{OH}	-	VDD-0.4	-	-	V
8	Output Low Voltage	V_{OL}	-	-	-	+0.4	V

4.3 Timming Characteristics

- Segment

(Segment Mode 1) (V_{SS} = V_5 = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 15.0 to +42.0 V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_R, t_F \leq 10ns$	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns	
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (V_{SS} = V_5 = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 15.0 to +42.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_R, t_F \leq 10ns$	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns	
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

5	Input High Voltage	V_{IH}	-	$0.8XV_{DD}$	-	V_{DD}	V
6	Input Low Voltage	V_{IL}	-	GND	-	$0.2XV_{DD}$	V
7	Output High Voltage	V_{OH}	-	VDD-0.4	-	-	V
8	Output Low Voltage	V_{OL}	-	-	-	+0.4	V

4.3 Timming Characteristics

- Segment

(Segment Mode 1) (V_{SS} = V_5 = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 15.0 to +42.0 V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_R, t_F \leq 10ns$	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns	
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (V_{SS} = V_5 = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 15.0 to +42.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_R, t_F \leq 10ns$	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns	
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

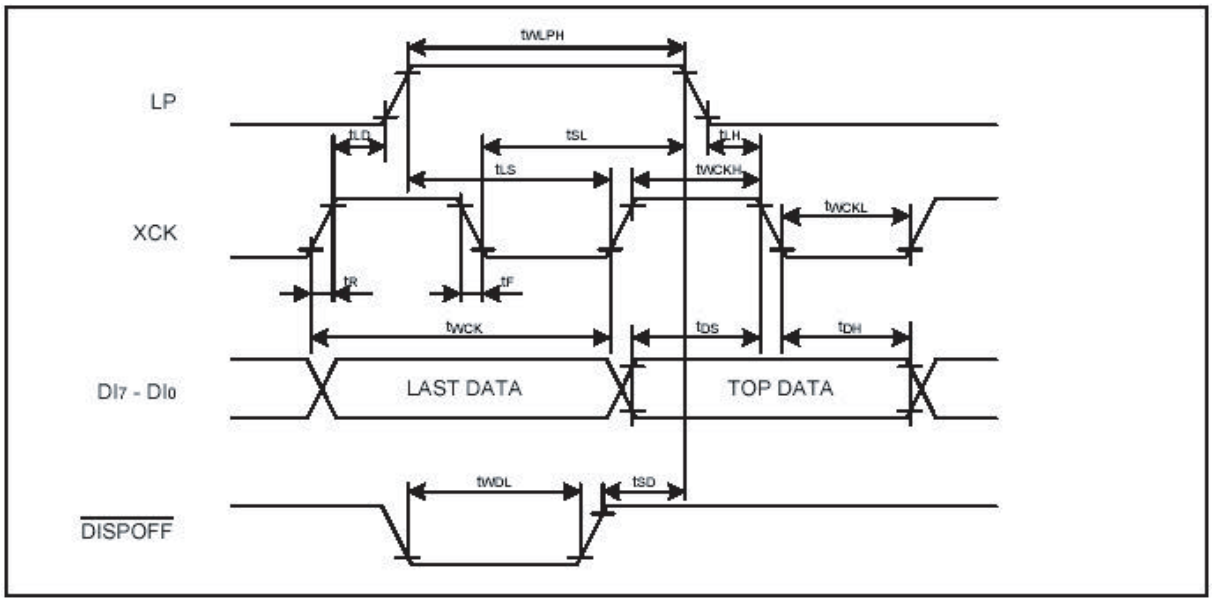
NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

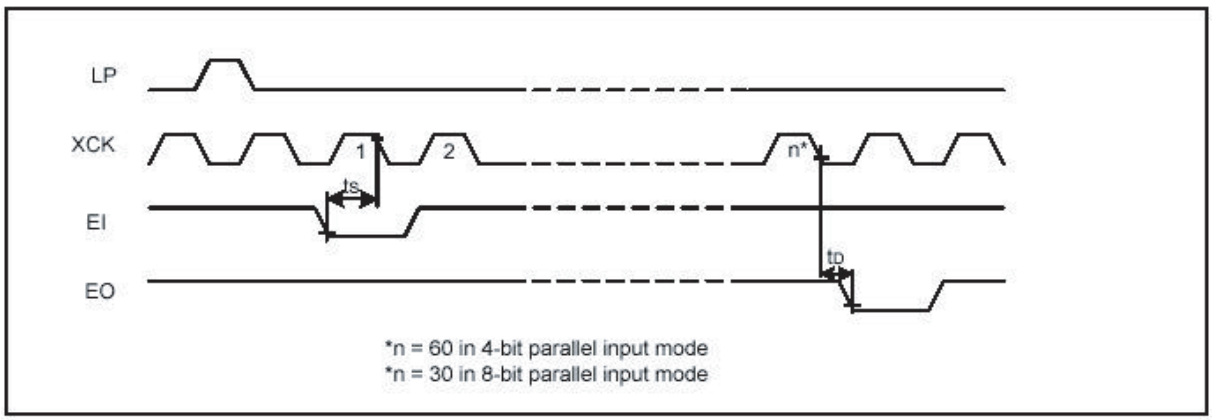
(Segment Mode 3) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = + 15.0 to +42.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		65			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns	
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.





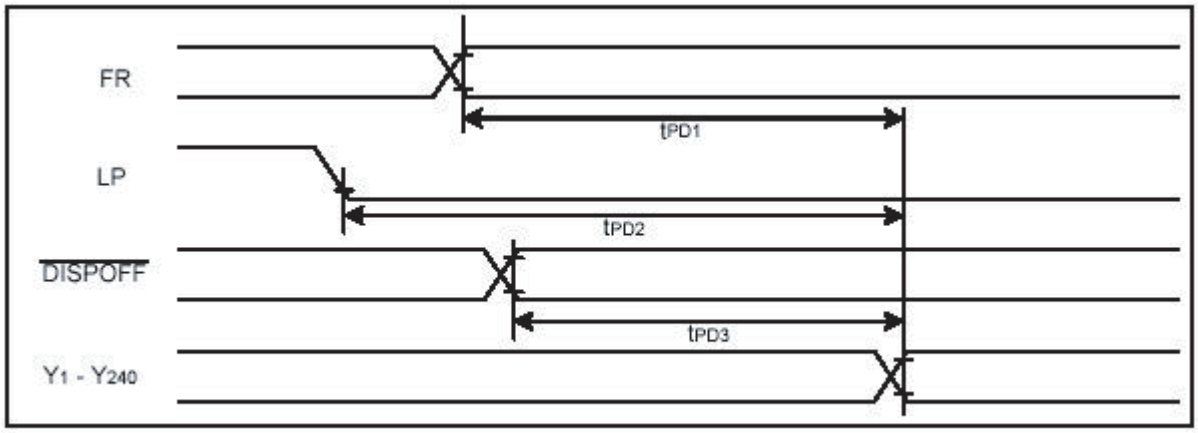
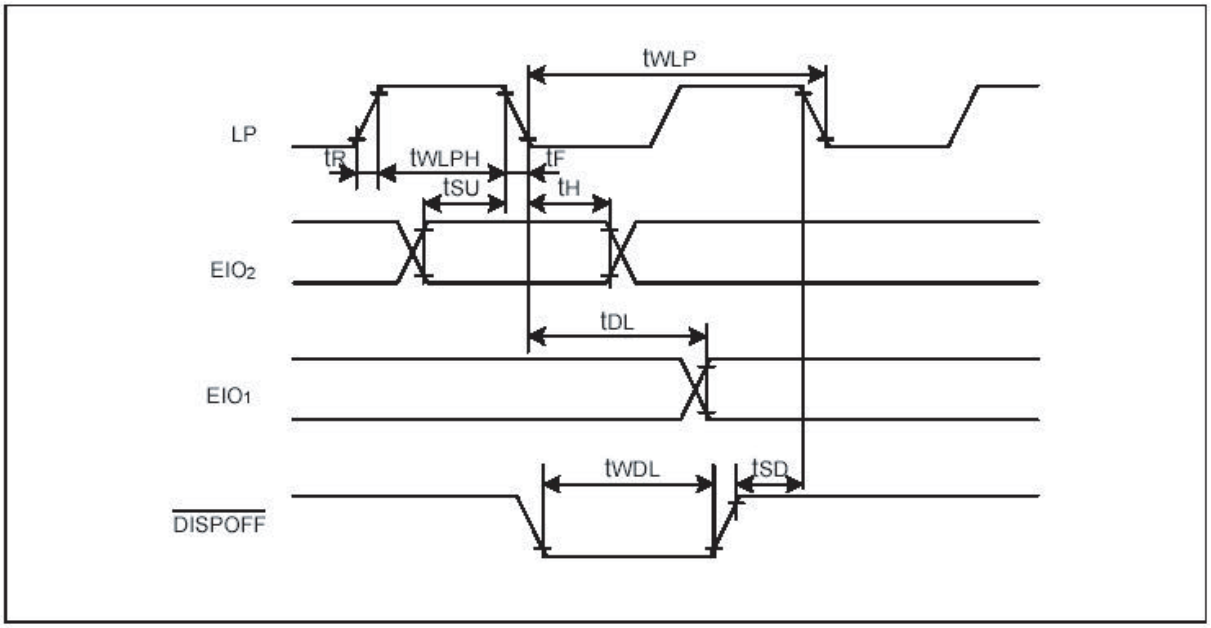


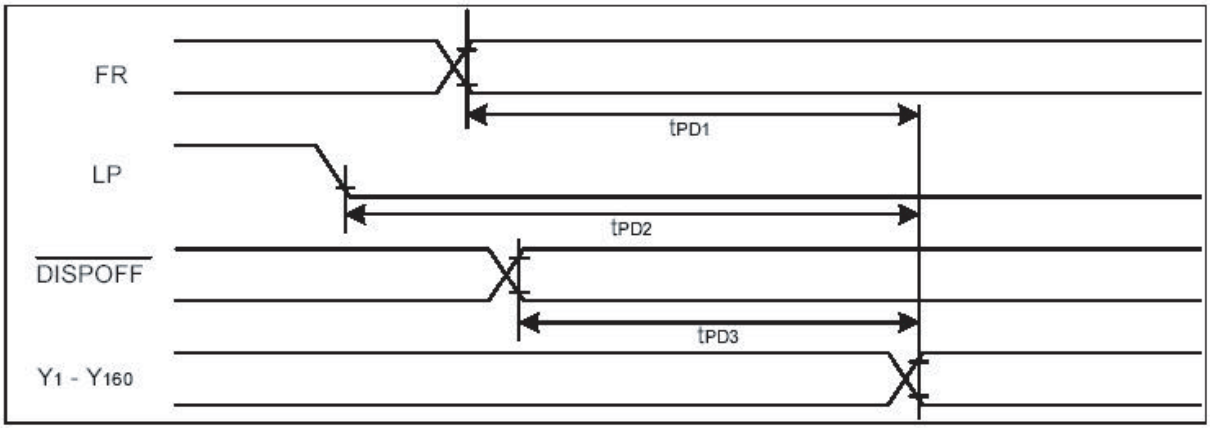
Fig. 8 Timing Characteristics (3)

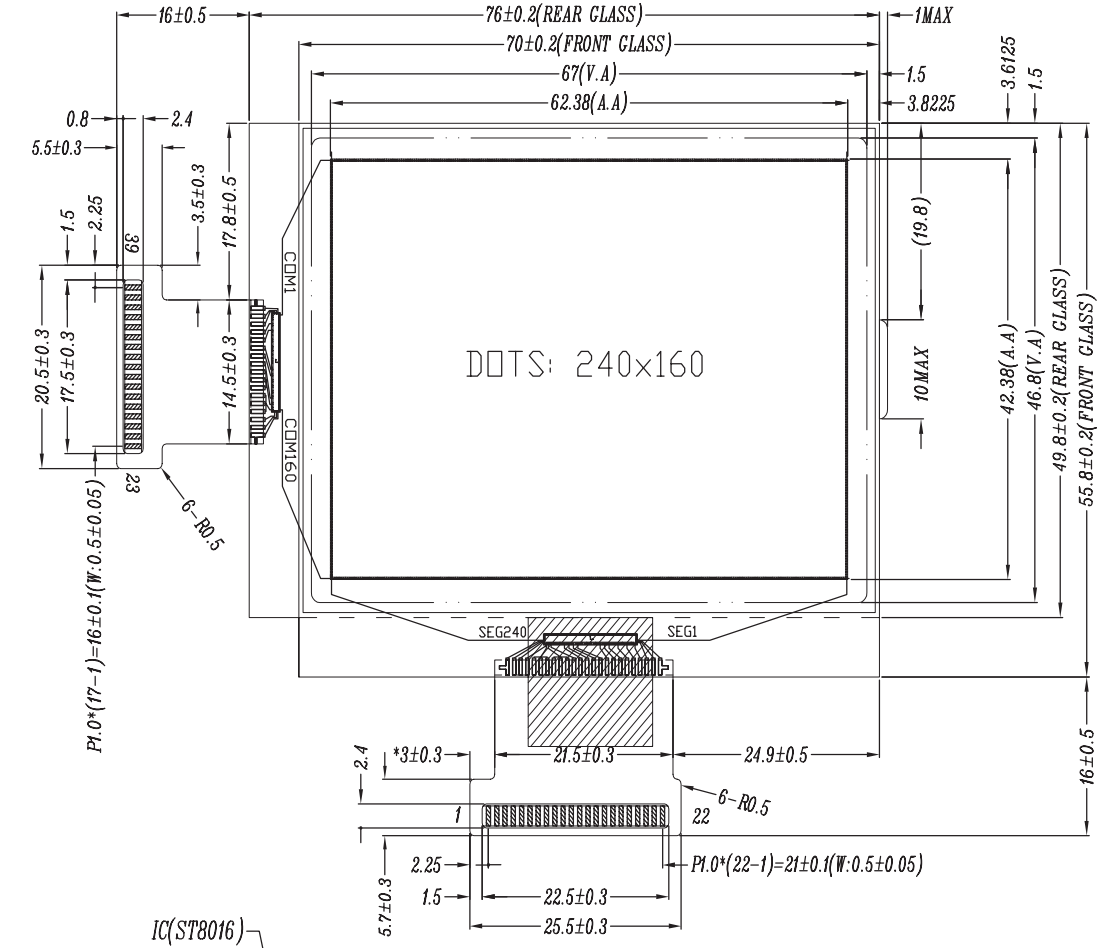
- **Common**

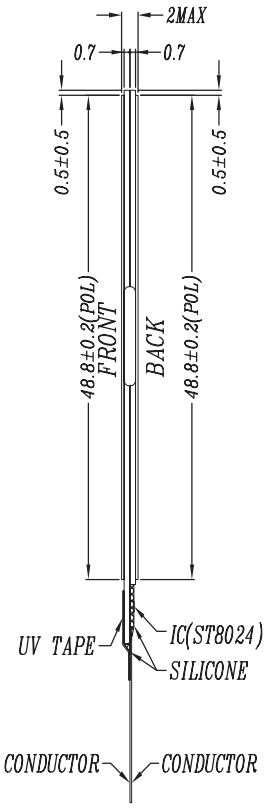
(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +30.0 V, T_{OPR} = -25 to +85° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R,t_F ≤ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0± 0.5V	15			ns
		V_{DD} = +2.5+ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs





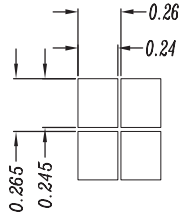




PIN DESCRIPTION

SEC		COM	
1	V0L	23	V0L
2	V12L	24	V12L
3	V34L	25	V34L
4	V5L	26	VSS
5	VSS	27	VSS
6	VSS	28	VSS
7	VDD	29	VDD
8	VDD	30	VDD
9	DBLKB	31	VDD
10	D0	32	EI02
11	D1	33	D7
12	D2	34	DOFF
13	D3	35	LP
14	XCK	36	FR
15	DOFFB	37	V34R
16	LP	38	V12R
17	FR	39	V0R
18	MD		
19	V5R		
20	V34R		
21	V12R		
22	V0R		

DOTS DETAIL
SCALE 20:1



NOTE:
1. DISPLAY TYPE: FSTN,TRANSFLECTIVE,POSITIVE,6:00
2. DRIVE METHOD: 1/160 DUTY,1/14 BIAS
3. OPERATING VOLTAGE: Vlcd=19.5V,VDD=5V
4. OPERATING TEMPERATURE: -10°~+60°
5. STORAGE TEMPERATURE: -20°~+70°
6. DRIVE IC: ST8024 & ST8016 (COG)
7. CONNECTOR: FPC
8. UNMARKED TOLERANCE: ±0.2

REVISION HISTORY	VERSION DESCRIPTION	DESIGNER	DATE
	A01:CORRECT THE MISTAKED VOP 9.5 TO BE 19.5. TURN OVER THE 'DOWN' FPC FROM LEFT TO RIGHT.	CZX	2005.06.16
	A00:Original Version	CBB	2005.06.04

CUSTOMER APPROVAL:

	DRAWN:	CHECKED:	QA CHECKED:	APPROVED:	AGM2416B	UNITS: mm
AZ DISPLAYS, INC.					DWG NO: ED-5130-LCM/A01	SHEET 1 OF 1