The Analog Mixed Signal Company

Data Sheet

Rev. 1.00 / April 2010

ZSSC3053

Pure Differential Sensor Signal Conditioner

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Brief Description

The ZSSC3053 is a CMOS integrated circuit for high-accurate amplification and sensor specific correction of mV-DC-sensor signals.

Featuring a programmable analog gain up to 420 digital processing allows for a maximum overall gain of 5000. Due to extended offset compensation capabilities the ZSSC3053 is adjustable to nearly all resistive bridge sensor types, e.g. piezo-resistive, thin-film and thick-film. It also enables the interfacing of single-ended resistive sensors (e.g. RTDs) or mV-DC-sources.

Digital compensation of offset, sensitivity, temperature drift and nonlinearity is accomplished by a 16-bit RISC microcontroller running a correction algorithm with calibration coefficients stored in an EEPROM.

Measured values are provided by digital interfaces I²C™ or SPI. In I²C™ mode two programmable switch outputs are available that indicate when the signal exceeds or falls below a programmable value. Since the calibration equipment and the ZSSC3053 are linked digitally noise sensitivity is greatly reduced. Digital calibration helps to keep assembly cost low as no trimming or laser tuning is needed.

For quick and easy evaluation and support of prototype calibration, ZMDI offers the ZSSC3053 Evaluation Kit, which includes an evaluation board, TSSOP14-samples and software.

Benefits

- Supports digital standard interfaces I²C™ & SPI with very low number of discrete external parts
- Complies to nearly all resistive sensor elements as well as to mV-DC-sources
- Single pass “one-shot” calibration minimizes calibration costs
- Two programmable switch outputs
- Programmable I²C™ slave address enables multi-slave-bus-operation

Physical Characteristics

- Supply voltage: (2.7 to 5.5) VDC
- Input signal span: 0.5 to 280 mV/V (minimum at max. digital gain)
- ADC resolution: 9 ~ 15 bits
- Output resolution: up to 15 bits
- Output data format: 16 bits
- TSSOP 14 package

Features

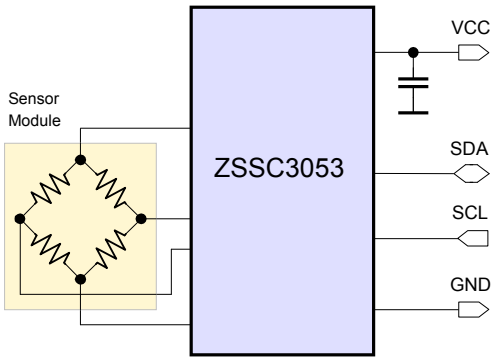
- Digital compensation of measured offset, gain, TC up to 2nd order, NL up to 3rd order
- Compensation of temperature sensor offset, gain, NL up to 2nd order
- Internal temperature reference
- Operational temperature range (-25 to +85)°C
- Accuracy: ±0.10% FSO @ (-25 to +85)°C
- 2 EEPROM words for user data

Applications & Examples

µC-based sensor systems in industrial, medical and consumer applications for measuring

- pressure
- temperature
- force & load
- linear position

ZSSC3053 Application Circuit



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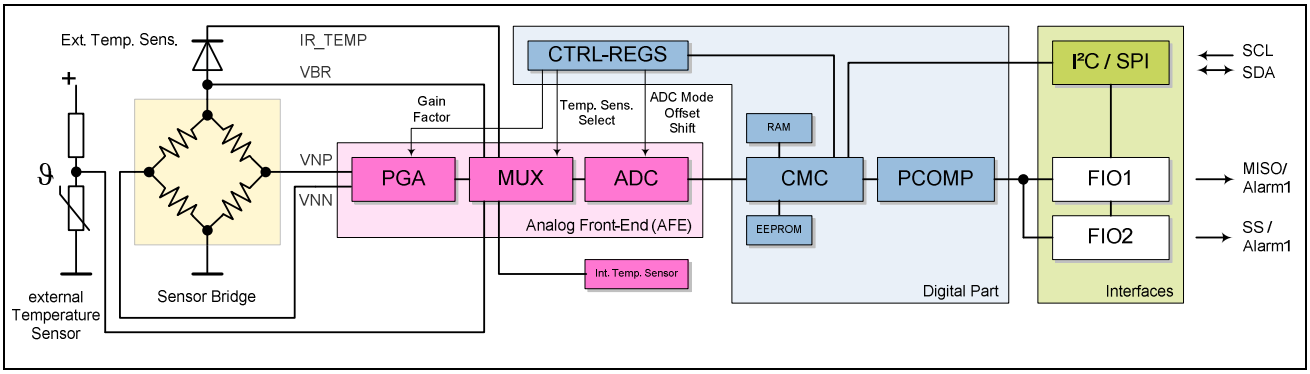
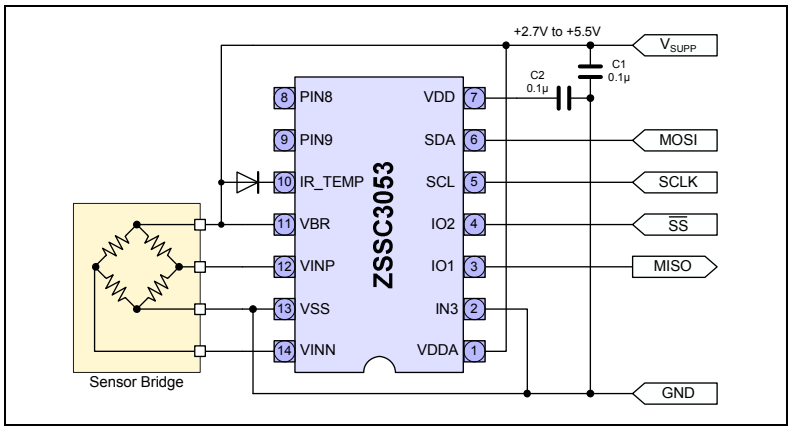
ZSSC3053 Block Diagram



Ratiometric Measurement



Ordering Information

Product Sales Code	Description	Package
ZSSC3053-ZI1R	ZSSC3053 – Pure Differential SSC	TSSOP14 (Tape & Reel)
ZSSC3053KIT Evaluation Kit V1.0	Modular evaluation and development boards for ZSSC3053	Kit boards, IC samples, USB cable, DVD with software and documentation

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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Table 1.1 Absolute Maximum Ratings

NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.1.1	Digital Supply Voltage	VDD_{AMR}	To VSS	-0.3		6.5	V DC
1.1.2	Analog Supply Voltage	$VDDA_{AMR}$	To VSS	-0.3		6.5	V DC
1.1.3	Voltage at all analog and digital I/O – Pins	$V_{A\_I/O}$, $V_{D\_I/O}$		-0.3		VDDA +0.3	V DC
1.1.4	Storage temperature	T_{STG}		-45		150	°C

1.2. Operating Conditions [1] (Voltages related to VSS)

Table 1.2 Operating Conditions

NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.2.1	Ambient temperature EEPROM programming	T_{AMB_EEP}		-25		85	°C
1.2.2	EEPROM programming cycles					100	
1.2.3	Data retention (EEPROM)		Average temp < 85°C			15	a
1.2.4	Analog Supply Voltage	VDDA		2.7		5.5	V DC
1.2.5	Analog Supply Voltage advanced performance	$VDDA_{ADV}$		4.5		5.5	V DC
1.2.6	Digital Supply Voltage	VDD	In case externally powered	- 2.7		1.05 -	VDDA V DC
1.2.7	Common mode input range	V_{IN_CM}	Depends on gain adjust, refer to chapter 2.3.1	0.21		0.76	V_{ADC_REF}
1.2.8	Sensor Bridge Resistance*	R_{BR}	Full temperature range	3.0 [2]		25.0	kΩ
1.2.9	Stabilization Capacitor *	C_{VDDA}	Between VDDA and VSS, external	50	100	470	nF
1.2.10	VDD Stabilization Capacitor *	C_{VDD}	Between VDD and VSS, external	0 [3]	100	470	nF

1 Configuration: 2nd order AD-conversion, 13 bit Resolution, gain ≥ 210, f_{clk} ≤ 2.25MHz
* Not tested in mass production, parameter is guarantied by design and/or quality monitoring
2 No limitations with an external connection between VDDA and VBR
3 Lower stabilization capacitors can increase noise level at the output

1.3. Build In Characteristics

Table 1.3 Build In Characteristics

NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.3.1	Selectable Input Span, Pressure Measurement	V_{IN_SP}	Utilizing full ADC Resolution, refer to chapter 2.3.1	2		280	mV/V
1.3.2	Analog Offset Comp (XZC) Range		6 Bit setting	-20		20	count
1.3.3	A/D Resolution	r_{ADC}	3 Bit setting [1]	9		15	Bit
1.3.4	Bias current for external temperature diodes	I_{TS}		8	18	40	µA
1.3.5	Sensitivity internal temperature diode	ST_{T_SI}	Raw values - without conditioning	2800	3200	3600	ppm f.s. /K
1.3.6	Clock frequency	f_{CLK}	guaranteed adjustment range	1 *	2	4 *	MHz

1.3.1. Cycle Rate versus A/D-Resolution *

(linear relation to master clock frequency - values calculated at exactly 2 MHz)

Table 1.4 Cycle Rate versus A/D-Resolution

ADC Order O_{ADC}	Resolution r_{ADC}	Conversion Cycle f_{CYC}	
		f_{CLK}=2MHz	f_{CLK}=2.25MHz
	[Bit]	[Hz]	[Hz]
1	9	1302	1465
	10	781	879
	11	434	488
	12	230	259
	13	115	129
	14	59	67
2	11	3906	4395
	12	3906	4395
	13	1953	2197
	14	1953	2197
	15	977	1099

[1] Resolution of 15 bits is not applicable for 1st order ADC and not recommended for sensors with high nonlinearity behavior
* Not tested in mass production, parameter is guarantied by design and/or quality monitoring

1.4. Electrical Parameters [1] (Voltages related to VSS)

Table 1.5 Electrical Parameters

NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.4.1. Supply / Regulation							
1.4.1.1	Supply current	I_{SUPP}	Without bridge and load current, $f_{CLK} \leq 2.4MHz$		2.5	4	mA
1.4.1.2	Temperature Coeff. Voltage Reference *	TC_{REF}		-200	±50	200	ppm/K
1.4.2. Analog Front End							
1.4.2.1	Parasitic differential input offset current *	I_{IN_OFF}	Temp. range 5.2.2., T_{ADV}	-2 ~ -10		2 ~ 10	nA
1.4.3. Temperature Sensors (Pin IR_TEMP)							
1.4.3.1	Sensitivity external diode / resistor meas.	ST_{TS_E}	at r_{ADC} = 13 Bit	75		210	µV/LSB
1.4.4. Digital Outputs (IO1, IO2)							
1.4.4.1	Output-High-Level	V_{DOUT_H}	R_L > 1 kΩ	0.9			VDDA
1.4.4.2	Output-Low-Level	V_{DOUT_L}	R_L > 1 kΩ			0.1	VDDA
1.4.5. System Response							
1.4.5.1	Startup time [2, *]	t_{STA}	Power On to 1st result at output	2		5	ms
1.4.5.2	Response time *	t_{RESP}	66% step, refer to 2.3.4 for f_{CON}	1.66	2.66	3.66	$1/f_{CON}$
1.4.5.3	Overall accuracy (deviation from ideal line including INL, gain and offset errors) *	AC_{OUT}	$VDDA_{ADV}$ VDDA			0.1 0.25	% %
1.4.5.4	Digital Output Noise		Shorted inputs, gain ≤ 210 bandwidth ≤ 10kHz [1]			1	LSB
1.4.5.5	Ratiometricity Error	RE_{OUT_5V}	VDDA = 5V ±5% VDDA = 5V ±10%			500 1000	ppm ppm
		RE_{OUT_3V}	VDDA = 3V ±5% VDDA = 3V ±10%			1000 2000	ppm ppm

1 Configuration: 2nd order AD-conversion, 13 bit Resolution, gain ≥ 210, $f_{clk} \leq 2.25MHz$
2 According default configuration (depends on resolution and configuration - start routine begins approximately 0.8ms after power on)
* Not tested in mass production, parameter is guarantied by design and/or quality monitoring

1.5. Interface Characteristics

Table 1.6. Interface Characteristics

NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
1.5.1. Multiport Serial Interfaces (I²C™, SPI)							
1.5.1.1	Input-High-Level	$V_{I^2C\_IN\_H}$		0.7		1	VDDA
1.5.1.2	Input-Low-Level	$V_{I^2C\_IN\_L}$		0		0.3	VDDA
1.5.1.3	Output-Low-Level	$V_{I^2C\_OUT\_L}$				0.1	VDDA
1.5.1.4	Load capacitance @ SDA	C_{SDA}				400	pF
1.5.1.5	Clock frequency SCL [1]	f_{SCL}	$f_{CLK} \geq 2MHz$			400	kHz
1.5.1.6	Pull-up Resistor	$R_{I^2C\_PU}$		500	5k		Ω
1.5.1.7	Input capacitance (each pin)	$C_{I^2C\_IN}$	valid for SPI as well			10	pF

[1] Internal clock frequency f_{CLK} has to be in minimum 5 times higher than communication clock frequency

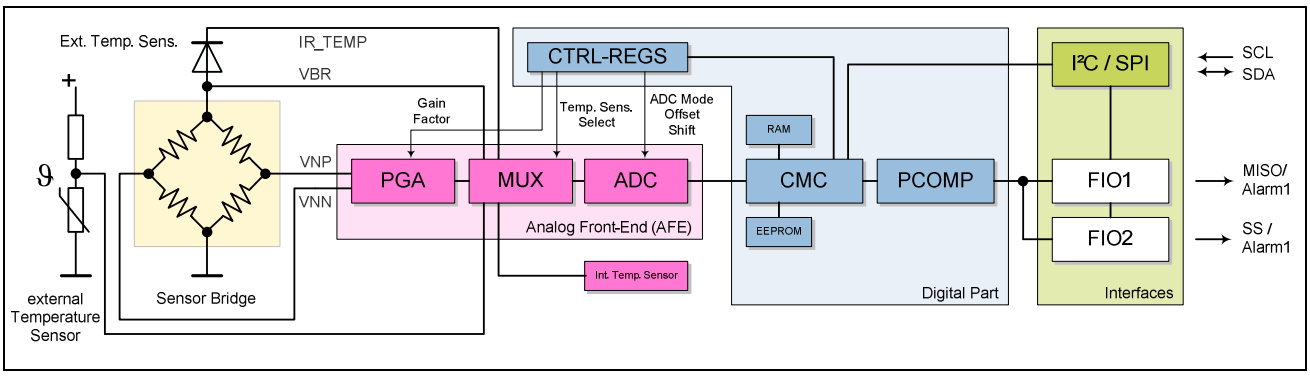
2 Circuit Description

2.1. Signal Flow

The ZSSC3053's contains an analog front-end (AFE) (pink) and a digital processing section (blue). The analog signal path is realized fully differential up to the A/D converter's input. The bridge sensor output is a differential signal with respect to a common mode potential (analog ground = VBR/2).

Consequently it is possible to amplify positive and negative input signals, as long as the common mode range is not exceeded (according to Table 2.1).

Figure 2.1 Block Diagram of the ZSSC3053



PGA ..... Programmable Gain Amplifier
MUX..... Multiplexer
ADC ..... Analog-to-Digital Converter
CMC ..... Calibration Microcontroller
FIO1..... Flexible I/O 1: SPI Data Out, Alarm1
FIO2..... Flexible I/O 2: SPI Slave Select , Alarm2
SIF ..... Serial interface: I^2C^{TM} Data I/O, SPI Data In, Clock
PCOMP ..... Programmable Comparator
EEPROM ..... Non Volatile Memory for Calibration Parameters and Configuration
TS ..... On-chip Temperature Sensor (pn-junction)
ROM ..... Memory for Correction Formula and –Algorithm

The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The Multiplexer (MUX) transmits the signals from bridge sensor, external diode or separate temperature sensor to the ADC in a sequence according to 2.3.3. The internal pn-junction (TS) can be used alternatively to the external diode. The ADC converts these signals into digital values.

The digital signal correction is performed in the calibration micro-controller (CMC). It is based on a special correction formula located in the ROM and on sensor-specific coefficients (stored into the EEPROM during calibration). Dependent on the programmed output configuration the corrected sensor signal is output in digital via SPI or I^2C^{TM} interface. The output switch signal is provided at 2 flexible I/O modules (FIO) additional. The configuration data and the correction parameters can be programmed into the EEPROM via the I^2C^{TM} interface.

2.2. Application Modes

For each application a configuration set has to be established (generally prior to calibration) by programming the on-chip EEPROM according to the following modes:

- Sensor channel
  - Sensor mode: ratiometric voltage
  - Input range: The gain of the analog front-end has to be chosen with respect to the maximum sensor signal span and to this has also adjusted the zero point of the ADC
  - Additional offset compensation: The extended analog offset compensation has to be enabled if required, i.e. if the sensor offset voltage is near to or larger than the sensor span.
  - Resolution/response time: The A/D converter has to be configured for resolution and conversion scheme (1st or 2nd order). These settings influence the sampling rate, signal integration time and thus the noise immunity.
  - Ability to invert the sensor bridge inputs
- Alarm output via IO1/2
- Digital communication: The preferred protocol and its parameter have to be set.
- Temperature
  - The temperature measurement source for the temperature correction has to be chosen.
  - The temperature measurement source T1 sensor type for the temperature correction has to be chosen (only T1 is usable for correction!)

Note: Not all possible combinations of settings are allowed (see section 2.5).

The calibration procedure must include

- Set of coefficients of calibration calculation

and, depending on configuration,

- Adjustment of the extended offset compensation,
- Zero compensation of temperature measurement,

and, if necessary,

- Set of thresholds and delays for the alarms.

2.3. Analog Front End (AFE)

The analog front end consists of the programmable gain amplifier (PGA), the multiplexer (MUX) and the analog-to-digital converter (ADC).

2.3.1. Programmable Gain Amplifier (PGA)

The following table shows the adjustable gains, the processable sensor signal spans and the allowed common mode range.

Table 2.1 Adjustable gains, resulting sensor signal spans, and common mode ranges

No.	PGA Gain a_{IN}	Gain Amp1	Gain Amp2	Gain Amp3	Max. span V_{IN_SP} in mV/V	Input range V_{IN_CM} in % VDDA *
1	420	30	7	2	2	43 - 57
2	280	30	4,66	2	3	40 - 59
3	210	15	7	2	4	43 - 57
4	140	15	4,66	2	6	40 - 59
5	105	15	3,5	2	8	38 - 62
6	70	7,5	4,66	2	12	40 - 59
7	52,5	7,5	3,5	2	16	38 - 62
8	35	3,75	4,66	2	24	40 - 59
9	26,3	3,75	3,5	2	32	38 - 62
10	14	1	7	2	50	43 - 57
11	9,3	1	4,66	2	80	40 - 59
12	7	1	3,5	2	100	38 - 62
13	2,8	1	1,4	2	280	21 - 76

2.3.2. Extended Zero Point Compensation (XZC)

The ZSSC3053 supports two methods of sensor offset cancellation (zero shift):

- Digital offset correction
- XZC – an analog cancellation for large offset values (up to approx 300% of span)

The digital sensor offset correction will be processed at the digital signal correction/conditioning by the CMC. The analog sensor offset pre-compensation will be needed for compensation of large offset values, which would overdrive the analog signal path by uncompensated amplification. For analog sensor offset pre-compensation a compensation voltage will be added in the analog signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits. It allows an analog zero point shift of up to 300% of the processable signal span.

The zero point shift of the temperature measurements can also be adjusted by 6 EEPROM bits (Z_{XZC}= -20…+20) and is calculated by:

$$V_{XZC} / VDD_{BR} = k * Z_{XZC} / (20 * a_{IN})$$

* Bridge in voltage mode

Table 2.2 Extended Zero Point Compensation Range

PGA Gain a_{IN}	Max. Span V_{IN_SP} [mV/V]	Calculation Factor k	Offset Shift per Step [% Full Span]	Approx. Maximum Offset Shift [mV/V]	Approx. Maximum Shift [% V_{IN_SP}] (@ ± 20 Steps)
420	2	3,0	15%	+/- 7	330
280	3	1,833	9%	+/- 6	200
210	4	3,0	15%	+/- 14	330
140	6	1,833	9%	+/- 12	200
105	8	1,25	6%	+/- 12	140
70	12	1,833	9%	+/- 24	200
52,5	16	1,25	6%	+/- 22	140
35	24	1,833	9%	+/-48	200
26,3	32	1,25	6%	+/- 45	140
14	50	3,0	15%	+/- 180	330
9,3	80	1,833	9%	+/- 160	200
7	100	1,25	6%	+/- 140	140
2,8	280	0,2	1%	+/- 60	22

Note: Z_{XZC} can be adjusted in range –31 to 31, parameters are guaranteed only in range –20 to 20.

2.3.3. Measurement Cycle realized by Multiplexer

The Multiplexer selects, depending on EEPROM settings, the following inputs in a defined sequence.

- Internal offset of the input channel measured by input short circuiting
- Bridge temperature signal measured by external and internal diode (pn-junction)
- Bridge temperature signal measured by bridge resistors
- Temperature measurement by external thermistor
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram on the right shows its principle structure.

The EEPROM adjustable parameters are:

- Pressure measurement count,

  PMC=<1, 2, 4, 8, 16, 32, 64, 128>
- Temperature 2 measurement enable,

  T2E=<0, 1>

After Power ON the start routine is called. It contains the pressure and auto zero measurement. When enabled it measures the temperature and its auto zeros.

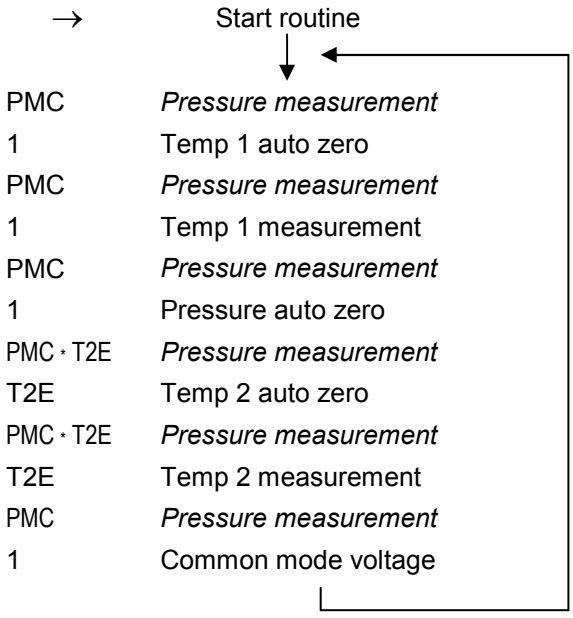


Figure 2.2. Measurement cycle ZSSC3053

2.3.4. Analog-to-Digital Converter

The ADC is a charge balancing converter in full differential switched capacitor technique. It can be used as first or second order converter:

In the **first order** mode it is inherently monotone and insensitive to short and long term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by:

$$t_{CYC\_1} = 2^{r_{ADC}}\ \mu s$$

The available ADC-resolutions are r_{ADC} = <9, 10, 11, 12, 13, 14> bits.

In the **second order** mode two conversions are stacked with the advantage of much shorter conversion cycle time and the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time in this mode is roughly calculated by:

$$t_{CYC\_2} = 2^{(r_{ADC}+3)/2}\ \mu s$$

The available ADC-resolutions are r_{ADC} = <11, 12, 13, 14, 15> bits.

The formulas give an overview about conversion time for one AD-conversion. Refer to calculation sheet "ZSSC3053_Bandwidth_Calculation_Rev*.xls" for detailed calculation of sampling time and bandwidth.

The result of the AD conversion is a relative counter result corresponding to the following equation:

$$Z_{ADC} = 2^{r_{ADC}} * [(V_{ADC\_DIFF} / V_{ADC\_REF}) + (1 - RS_{ADC})]$$

Z_{ADC}: Number of counts (result of the conversion)

V_{ADC_DIFF}: Differential input voltage of ADC (= a_{IN} * V_{IN_DIFF})

V_{ADC_REF}: Reference voltage of ADC (= VBR or VDDA)

RS_{ADC}: Digital ADC Range Shift (RS_{ADC} = $^{15}/_{16}$, $^{7}/_{8}$, $^{3}/_{4}$, $^{1}/_{2}$, controlled by the EEPROM content)

With the RS_{ADC} value a sensor input signal can be shifted to the optimal input range of the ADC.

The Pin <VBR>-potential is used in "VBR=VREF" mode as the A/D converter's reference voltage V_{ADC_REF}.
Note: The AD conversion time (sample rate) is only a part of a whole signal conditioning cycle.

Table 2.3 Output Resolution versus Sample Rate

ADC Order O_{ADC}	Maximum Output Resolution		Sample Rate f_{CON}	
	r_{ADC} [1]	Digital-OUT	f_{CLK}=2MHz	f_{CLK} =2.25MHz
	[Bit]	[Bit]	[Hz]	[Hz]
1	9	9	1302	1465
	10	10	781	879
	11	11	434	488
	12	12	230	259
	13	13	115	129
	14	14	59	67

[1] *ADC Resolution should be 1 to 2 bits higher then applied Output Resolution*

ADC Order O_{ADC}	Maximum Output Resolution		Sample Rate f_{CON}	
	r_{ADC} [1]	Digital-OUT	f_{CLK}=2MHz	f_{CLK} =2.25MHz
	[Bit]	[Bit]	[Hz]	[Hz]
2	10	10	3906	4395
	11	11	3906	4395
	12	12	3906	4395
	13	13	1953	2197
	14	14	1953	2197
	15	15	977	1099

2.4. System Control

The system control has the following features:

- Control of the I/O relations and of the measurement cycle according to the configuration data stored in EEPROM
- 16 bit correction calculation for each measurement signal using the calibration coefficients stored in the EEPROM and ROM-based algorithms
- It is started by internal POC, internal clock – generator or external clock
- For safety improvement the EEPROM data is checked with a signature during initialization procedure, the registers of the CMC are steadily observed with a parity check. Once an error is detected, the error flag of the CMC is set and the outputs are driven to a diagnostic value.

Note: The conditioning includes up to third order sensor input correction. The available adjustment ranges depend on the specific calibration parameters, a detailed description will be provided on request. Basic considerations are: Offset compensation and linear correction are only limited by a loss of resolution they may cause, the second order correction is possible up to about 20% full scale difference to straight line, third order up to about 10% (ADC resolution = 13bit). The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution influences also calibration possibilities – 1 bit higher resolution results in approximately half the calibration range.

2.5. Output Stage

The ZSSC3053 provides the following I/O pins: IO1, IO2, SCL and SDA for SPI and I²C™ communication as well as switch signal outputs (called ALARM).

Table 2.4. Output Configurations Overview

No.	Used SIF		Used I/O pins			
	I²C™	SPI	IO1	IO2	SCL	SDA
1	X				SCL	SDA
2	X		ALARM1		SCL	SDA
3	X			ALARM2	SCL	SDA
4	X		ALARM1	ALARM2	SCL	SDA
5		X	MISO	Slave select	SCK	MOSI
6		X	MISO ALARM1	Slave select	SCK	MOSI
7		X	MISO	Slave select	SCK	MOSI

Note: The Alarm signal only refers to the bridge sensor signal, but not to a temperature signal. In the SPI mode the pin IO2 is used as Slave Select. Thus no Alarm 2 can be output in this mode

2.5.1. Comparator Module (ALARM Output)

The comparator module consists of two digital comparators switchable to IO1 and IO2. Each of them can be independently programmed referring to the parameters threshold, hysteresis, switching direction and on/off – delay. Additionally a window comparator mode is available.

2.5.2. Serial Digital Interface

The ZSSC3053 includes a serial digital interface which is able to communicate based on two different communication protocols – I²C™ and SPI™.

In the SPI mode the pin IO2 operates as slave select input (SS), the pin IO1 as data output (MISO).

Initializing Communication

The serial interface switches to I²C™ or SPI mode after power on, depending on EEPROM settings.

2.6. Watchdog and Error Detection

The ZSSC3053 detects various possible errors. A detected error is signalized by changing in a diagnostic mode. In this case the analog output is set to the high or low level (maximum or minimum possible output value) and the output registers of the digital serial interface are set to a significant error code. A watchdog monitors the continuous working operation of the CMC and the running measurement loop. A check of the sensor bridge for broken wires is done permanently by two comparators watching the input voltage of each input [(VSSA + 0.5V) to (VDDA – 0.5V)]. Additionally on the common mode voltage of the sensor is watched permanently (sensor aging). Different functions and blocks in digital part are monitored continuously such as RAM-, ROM-, EEPROM- and Register content.

3 Application Circuit Examples

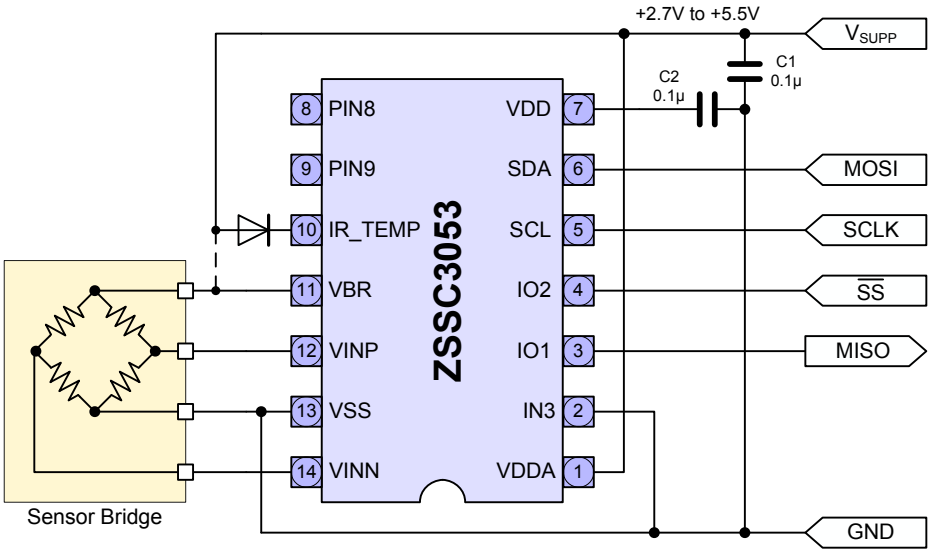


Figure 3.1 Application Example

Ratiometric measurement with digital SPI output, temperature compensation via external diode (bridge can be, but does not necessarily have to be connected to VDDA)

4 ESD/Latch-Up-Protection

All pins have an ESD protection of >2000V (except the pins INN, INP, PIN8 and PIN9 with > 1200V) and a latch-up protection of ±100mA or of +8V/ –4V (to VSS/VSSA) – refer to chapter 5 for details and restrictions. ESD protection referred to the human body model is tested with devices in TSSOP14 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, method 3015.7.

5 Pin Configuration and Package

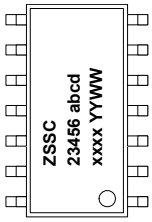
Table 4.1. Pin Configuration

Pin	Name	Description	Remarks	Latch-up Related Application Circuit Restrictions and/or Remarks
1	VDDA	Positive analog supply voltage	Supply	
2	IN3	Resistive temp sensor IN & external clock IN	Analog IN	
3	IO1	SPI data out & ALARM1	Digital IO	
4	IO2	SPI chip select & ALARM2	Digital IO	
5	SCL	I²C clock & SPI clock	Digital IN, pull-up	
6	SDA	Data-I/O @ I²C / Data-IN @ SPI	Digital I/O, pull-up	
7	VDD	Internally generated digital supply voltage	Supply	Only capacitor to VSS allowed, otherwise no application access
8	PIN8	Pin 8	Short to PIN9	Not use
9	PIN9	Pin 9	Short to PIN8	Not use
10	IR_TEMP	Temperature diode in	Analog I/O	Circuitry secures potential inside of VSS-VDDA range, otherwise no application access
11	VBR	Positive supply voltage	Analog I/O	Only short to VDDA or connection to sensor bridge, otherwise no application access
12	VINP	Positive input sensor bridge	Analog IN	
13	VSS	Negative supply voltage	Ground	
14	VINN	Negative input sensor bridge	Analog IN	

The standard package of the ZSSC3053 is a TSSOP14 (4.4mm body width) with lead-pitch 0.65mm.

Figure 4.1. Pin Configuration

Pin No.	Pin Name		Pin Name	Pin No.
8	PIN8		VDD	7
9	PIN9		SDA	6
10	IR_TEMP		SCL	5
11	VBR		IO2	4
12	VINP		IO1	3
13	VSS		IN3	2
14	VINN		VDDA	1



6 Reliability

A reliability investigation according to the in-house non-automotive standard will be performed.

A FIT rate < 5FIT (temp=55°C, S=60%) is guaranteed. A typical FIT rate of the C7A technology, which is used for ZSSC3053, is 2.5FIT.

7 Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZSSC3053, ZMDI can customize the circuit design by adding or removing certain functional blocks.

ZMDI owns a considerable library of sensor-dedicated circuit blocks for this purpose.

Thus ZMDI can provide a custom solution quickly. Please contact ZMDI for further information.

8 Ordering Information

Product Sales Code	Description	Package
ZSSC3053-ZI1R	ZSSC3053 – Pure Differential SSC	TSSOP14 (Tape & Reel)
ZSSC3053KIT Evaluation Kit V1.0	Modular evaluation and development boards for ZSSC3053	Kit boards, IC samples, USB cable, DVD with software and documentation

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for detailed informations and the latest version of this documents.

9 Glossary

Term	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front End
CMC	Calibration Microcontroller
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Device
FSO	Full Scale Output
INL	Integral Nonlinearity
MUX	Multiplexer
PGA	Programmable Gain Amplifier
PMC	Pressure Measurement Count
POC	Power On Control
SIF	Serial Interface
T2E	Temperature 2 Measurement
XZC	Extended Zero Point Compensation

10 Document Revision History

Revision	Date	Description
1.00	09. April 2010	First release of document.

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