ZMD31150

Fast Automotive Sensor Signal Conditioner

Datasheet PRELIMINARY

Features

- Digital compensation of sensor offset, sensitivity, temperature drift and non-linearity
- Adjustable to nearly all bridge sensor types, analog gain: 420, over all gain: up to 2000
- Output options: analog voltage (0...5V) or ZACwire™ (digital one-wire-interface)
- Temperature compensation: internal or external diode, bridge resistance, thermistor
- Sensor biasing by voltage or constant current
- Sample rate up to 7.8kHz
- High voltage protection up to 33V
- Reverse polarity and short circuit protection
- Wide operation temperature –40...+150°C
- Supply voltage 4.5...5.5V
- Product traceability by user-defined EEP entries
- Several safety- and diagnostic functions

Benefits

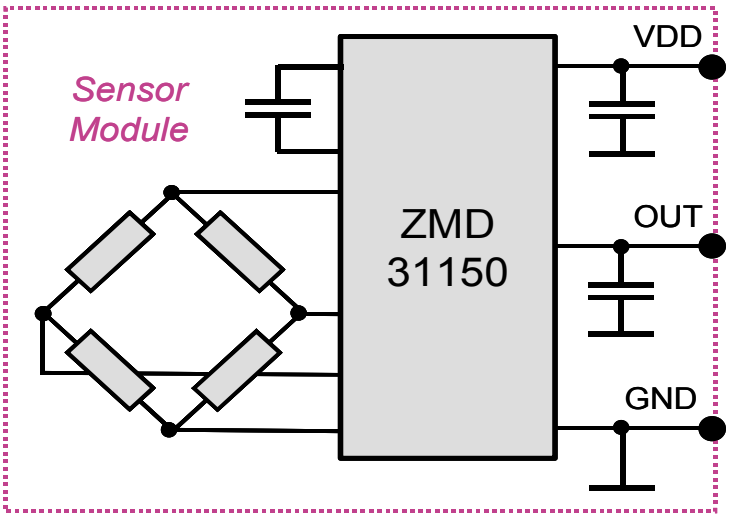
- No external trimming components required
- PC-controlled configuration and One-Shot calibration via one-wire interface: simple, low cost, quick and precise
- End-of-Line calibration via one-wire-interface
- High accuracy (0.25% FSO @ -25 to 85°C; 0.5% FSO @ -40 to 125°C)

Brief Description

ZMD31150 is a CMOS integrated circuit for highly-accurate amplification and sensor-specific correction of bridge sensor signals. Digital compensation of sensor offset, sensitivity, temperature drift and non-linearity is accomplished via a 16-bit RISC micro-controller running a correction algorithm with calibration coefficients stored in an EEPROM.
The ZMD31150 is adjustable to nearly all bridge sensor types. Measured values are provided at the analog voltage output or at the digital ZACwire™ and I²C interface. The digital interface can be used for a simple PC-controlled calibration procedure, in order to program a set of calibration coefficients into an on-chip EEPROM. Thus a specific sensor and a ZMD31150 are mated digitally: fast, precise and without the cost overhead associated with trimming by external devices or laser.

The ZMD31150 is optimized for automotive environments by it's special protection circuitry and excellent electromagnetic compatibility.

- **Evaluation kit available with samples**
- **Mass calibration solution**
- **Customization possible for large**



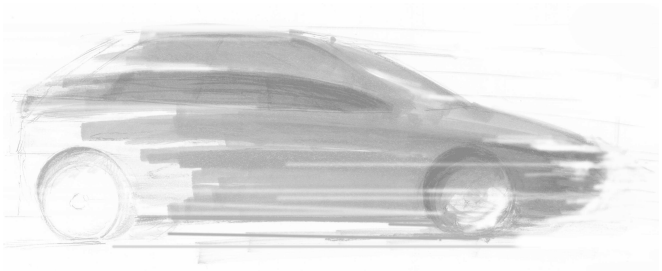


Fig 1: Sensor Module Schematic

ZMD31150

Advanced Automotive Sensor Signal Conditioner

Datasheet PRELIMINARY

Contents

1. Circuit Description

1.1 Signal Flow

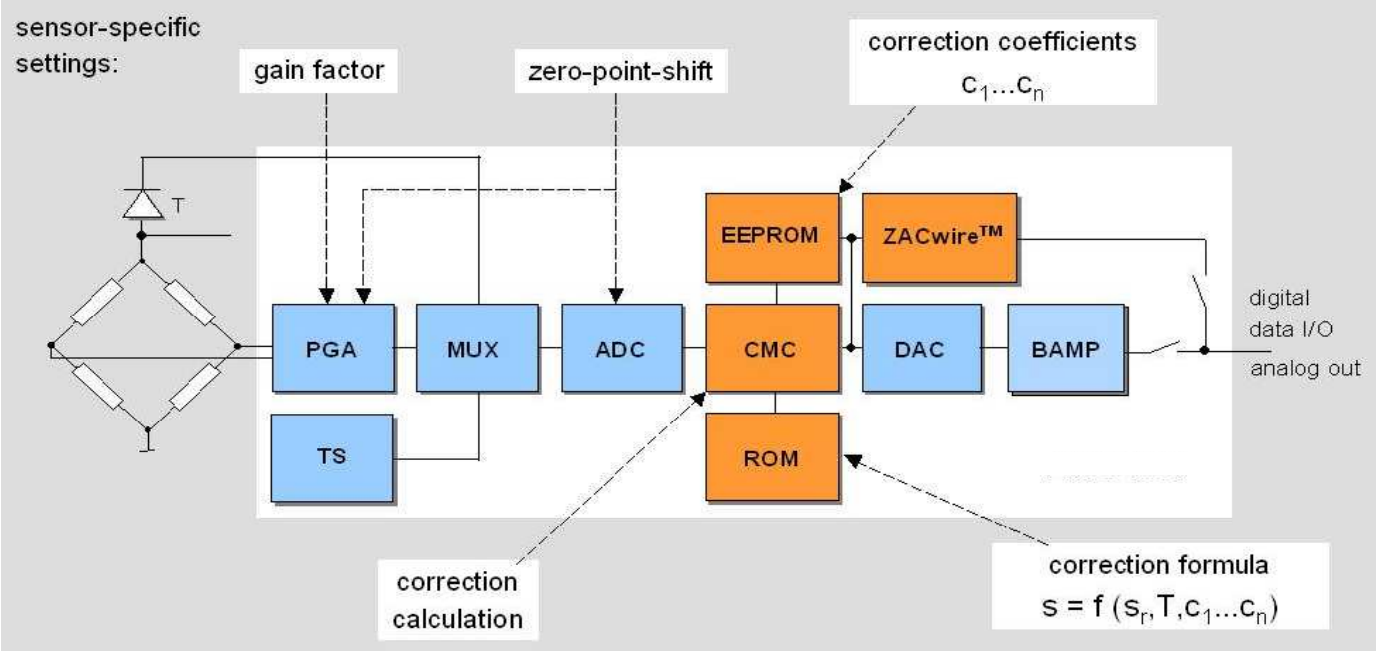


Fig.2: Block diagram of ZMD31150

The ZMD31150's signal path is partly analog (blue) and partly digital (red). The analog part is realized differential – this means the differential bridge sensor signal is internal handled via two signal lines, which are rejected symmetrically around a common mode potential (analog ground = VDDA/2). Consequently it is possible to amplify positive and negative input signals, which are located in the common mode range of the signal input.

The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The Multiplexer (MUX) transmits the signals from bridge sensor, external diode or separate temperature sensor to the ADC in a certain sequence (instead of the temp. diode the internal pn-junction (TS) can be used optionally). Afterwards the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration micro-controller (CMC). It is based on a correction formula located in the ROM and on sensor-specific coefficients (stored into the EEPROM during calibration). Dependent on the programmed output configuration the corrected sensor signal is output as analog value or in digital format (I^2C, ZACwire™). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

1.2 Application Modes

For each application a configuration set has to be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

- **Sensor channel**
  - **Sensor mode**: ratiometric bridge excitation in voltage or current supply mode.
  - **Input range**: the gain adjustment of the AFE with respect to the maximum sensor signal span and the zero point of the ADC has to be chosen
  - **Additional offset compensation XZC**: the extended analog offset compensation has to be enabled if required, e.g. if the sensor offset voltage is near to or larger than the sensor span.
  - **Resolution/response time**: the A/D converter has to be configured for resolution and converting scheme or **ADC Order** (first or second order). These settings influence the sampling rate, signal integration time and this way the noise immunity.
- **Temperature**
  - **Temperature measurement**: the source for the temperature correction has to be chosen.

1.3 Analog Front End (AFE)

The analog front end consists of the PGA, the MUX and the ADC.

1.3.1. Programmable Gain Amplifier

Table 1 shows the adjustable gains, the sensor signal spans and the allowed common mode range.

No.	overall gain a_{IN}	Max. span V_{IN_SP} [mV/V]	Gain Amp1	Gain Amp2	Gain Amp3	Max. span V_{IN_SP} [mV/V] *	Input common mode range V_{IN_CM} in % VDDA *	
							XZC=off	XZC=on
1	420	2	30	7	2	1,8	29 … 65	45…55
2	280	3	30	4,66	2	2,7	29 … 65	45…55
3	210	4	15	7	2	3,6	29 … 65	45…55
4	140	6	15	4,66	2	5,4	29 … 65	45…55
5	105	8	7,5	7	2	7,1	29 … 65	45…55
6	70	12	7,5	4,66	2	10,7	29 … 65	45…55
7	52,5	16	3,75	7	2	14,3	29 … 65	45…55
8	35	24	3,75	4,66	2	21,4	29 … 65	45…55
9	26,3	32	3,75	3,5	2	28,5	29 … 65	45…55
10	14	50	1	7	2	53,6	29 … 65	45…55
11	9,3	80	1	4,66	2	80	29 … 65	45…55
12	7	100	1	3,5	2	107	29 … 65	45…55
13	2,8	280	1	1,4	2	267	32 … 57	

Table 1: Adjustable gains, resulting sensor signal spans and common mode ranges

* Bridge in voltage mode, containing maximum input signal (with XZC: +300% Offset), 14bit accuracy
refer "ZMD31150 Functional description" for usable input signal/common mode range at bridge in current mode

1.3.2. XZC - Analog Sensor Offset Compensation

The ZMD31150 supports two methods of sensor offset compensation (zero shift):

- digital offset correction
- XZC - analog compensation for large offset values
  (up to in maximum approximately 300% of span, depending on gain adjustment)

Digital sensor offset correction will be processed at the digital signal correction/conditioning by the CMC. Analog sensor offset pre-compensation will be needed for compensation of large offset values, which would be overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation a compensation voltage will be added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits.

PGA gain a_{IN}	Max. span V_{IN_SP} in mV/V	Offset shift per step in % full span	Approx. maximum offset shift in mV/V	Approx. maximum shift in [% V_{IN_SP}] (@ ± 31)
420	2	12,5%	7,8	388%
280	3	7,6%	7,1	237%
210	4	12,5%	15,5	388%
140	6	7,6%	14,2	237%
105	8	5,2%	13	161%
70	12	7,6%	28	237%
52,5	16	5,2%	26	161%
35	24	7,6%	57	237%
26,3	32	5,2%	52	161%
14	50	12,5%	194	388%
9,3	80	7,6%	189	237%
7	100	5,2%	161	161%
2,8	280	0,83%	72	26%

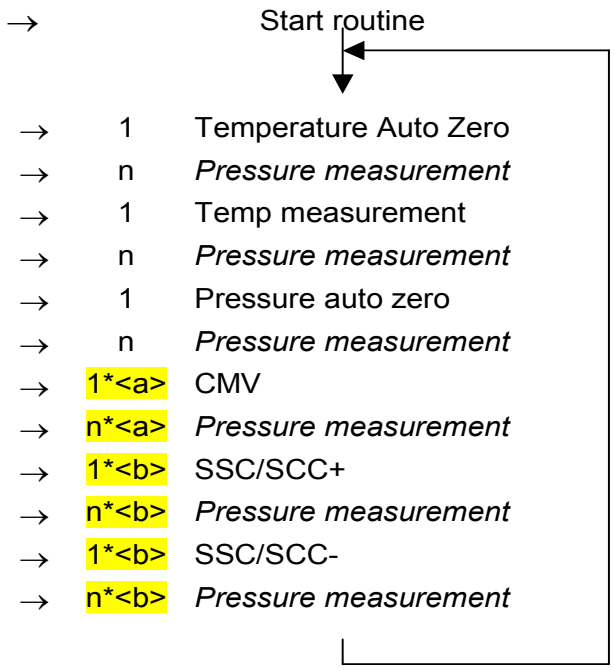
Table 2: Analog Zero Point Shift Ranges

1.3.3. Measurement Cycle

The Multiplexer selects, depending on EEPROM settings, the following inputs in a certain sequence.

- Temperature measured by external diode or thermistor, internal pn-junction or bridge
- Internal offset of the input channel
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram at the right shows its principle structure.



The EEPROM adjustable parameters are:

- n=<1,32>: Pressure measurement count
- a=<0,1>: CMV measurement enable
- b=<0,1>: SSC/SCC meas. enable

After power on the start routine is called, which contains all needed measurements once.

1.3.4. Analog-to-Digital Converter

The ADC is an integrating AD-Converter in full differential switched capacitor technique.

Programmable ADC-resolutions are r_{ADC}=<13,14> and <15,16> bit.

It can be used as first or second order converter. In the **first order** mode it is inherently monotone and insensitive against short and long term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by:

$$t_{CYC\_1} = 2^{r}\ \mu s / 2 / f_{CLK}$$

In the **second order** mode two conversions are stacked with the advantage of much shorter conversion cycle time and the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time at this mode is roughly calculated by:

$$t_{CYC\_2} = 2^{(r+3)/2} / 2 / f_{CLK}$$

The calculation formulas give a overview about conversion time for one AD-conversion. Refer Calculation sheet “ZMD31150_Bandwidth_Calculation_Rev*.xls” for detailed calculation of sampling time and bandwidth.

The result of the AD conversion is a relative counter result corresponding to the following equation:

$$Z_{ADC} = 2^{r} * (V_{ADC\_DIFF} / V_{ADC\_REF} - RS_{ADC})$$

Z_{ADC}: number of counts (result of the conversion)
r: adjusted resolution in bit
V_{ADC/REF_DIFF}: differential input/reference voltage of ADC
RS_{ADC}: digital ADC Range Shift (RS_{ADC} = $^{1}/_{16}$, $^{1}/_{8}$, $^{1}/_{4}$, $^{1}/_{2}$, controlled by the EEPROM content)

With the RS_{ADC} value a sensor input signal can be shifted in the optimal input range of the ADC.

ADC Adjustment		approx. Output Resolution *1)		Sample Rate f_{CON} *2)		Averaged Bandwidth @	
Order	r_{ADC}	Digital	Analog	f_{CLK}=3MHz	f_{CLK}=4MHz	f_{CLK}=3MHz	f_{CLK}=4MHz
O_{ADC}	Bit	Bit	Bit	Hz	Hz	Hz	Hz
1	13	13	12	345	460	130	172
1	14	14	12	178	237	67	89
1	15	14	12	90	120	34	45
1	16	14	12	45	61	17	23
2	13	13	12	5859	7813	2203	2937
2	14	14	12	3906	5208	1469	1958
2	15	14	12	2930	3906	1101	1468
2	16	14	12	1953	2604	734	979

Table 3: Output resolution versus sample rate

**1) ADC resolution should be one bit higher then applied output resolution, if AFE gain is adjusted in such manner, that input range is used more than 50%. Otherwise ADC resolution should be more than one bit higher than applied output resolution.*
**2) The sampling rate (AD conversion time) is only a part of the whole cycle, refer "ZMD31150 bandwidth calculation sheet" for detailed information*

1.4 Temperature Measurement

The ZMD31150 supports four different methods for temperature data acquiring needed for calibration of the sensor signal in temperature range. Temperature data can be acquired using:

- an internal pn-junction temperature sensor,
- an external pn-junction temperature sensor connected to sensor top potential (VBRTOP),
- an external resistive half bridge temperature sensor and
- the temperature coefficient of the sensor bridge at bridge current excitation.

Refer "ZMD31150 Functional Description" for a detailed explanation of temperature sensor adaptation and adjustment.

1.5 System Control and Conditioning Calculation

The system control has the following features:

- control the measurement cycle regarding to the EEPROM-stored configuration data
- 16 bit correction calculation for each measurement signal using the EEPROM stored calibration coefficients and ROM-based algorithms = signal conditioning
- manage start up sequence and start signal conditioning
- handle communication requests received by the serial interface
- process safety checks of digital and analog parts of the ZMD31150 and message detected errors with diagnostic states

Refer "ZMD31150 Functional Description" for a detailed description of system control and conditioning equation.

1.5.1. Operation Modes

The internal state machine represents three main states:

- the continuous running signal conditioning mode – called **N**ormal **O**peration **M**ode: NOM
- the calibration mode with access to all internal registers and states – called **C**ommand **M**ode: CM
- the failure messaging mode – called **D**iagnostic **M**ode: DM

1.5.2. Start Up Phase

The start up phase consist of following parts:

- internal supply voltage settling phase – finished by disabling the reset signal through the power on clear block (POC)
- set up the system control, read out and verifying the EEPROM and ROM content
- processing the start routine of signal conditioning (measure all needed data once, calculate the signal conditioning equation result first time)

The analog output AOUT is switched "tristate" during this and will be activated at the end of start up phase depending on adjusted output and communication mode (1.6). In case of detected errors Diagnostic Mode (DM) is activated and diagnostic output signal is driven at the output.

After the start up phase the continuous running calibration cycle is started.

1.5.3. Conditioning Calculation

The digitalized value for pressure (acquired raw data) is processed with the correction formula to remove offset and temperature dependency and to compensate non-linearity up to 3rd order. The result of the correction calculation is a non-negative 15 Bit value for pressure (P) in the range [0; 1). This value P is clipped with programmed limitation coefficients and continuously written to the output register of the digital serial interface and the output DAC.

Note: The conditioning includes up to third order nonlinearity sensor input correction. The available adjustment ranges depend on the specific calibration parameters, for a detailed description refer to "ZMD31150 Functional Description". To give a rough idea: Offset compensation and linear correction are only limited by the loose of resolution it will cause, the second order correction is possible up to about 30% full scale difference to straight line, third order up to about 20% (ADC resolution = 13bit). The used calibration principle is able to reduce present nonlinearity errors of the sensor up to 90%. The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution influences also calibration possibilities – 1 bit more resolution reduces calibration range by

approximately 50%. Calculation input data width is in maximum 14bit. 15 & 16bit ADC resolution mode uses only a 14 bit segment of ADC range.

1.6 Analog Output AOUT

The analog output is used for output the analog signal conditioning result and for "End of Line" communication via the ZACwire™ interface (one wire communication interface - OWI). The ZMD31150 supports four different modes of the analog output in combination with OWI behavior:

- OWI for ever: AOUT is used always for communication, no analog output is active
- OWI disabled: no communication via the analog output AOUT
- OWI window: communication via AOUT is enabled for a start window, after this AOUT is active
- AOUT & OWI window:
  analog output at AOUT is active after start up phase, OWI start window is parallel open for 100ms, to communicate the internal driven potential at AOUT has to be overwritten by the external communication master (AOUT drive capability is current limited)

The analog output potential is driven by an unity gain output buffer, those input signal is generated by an 12bit resistor string DAC. The output buffer (BAMP) – a rail-to-rail OPAMP - is offset compensated and current limited. So a short circuit of analog output against ground or power supply does not damage the ZMD31150.

1.7 Serial Digital Interface

The ZMD31150 includes a serial digital interface (SIF), which is used for communication with the circuit to realize calibration of the sensor module. The serial interface is able to communicate with two communication protocols – I^2C™ and ZACwire™ (one wire communication interface - OWI). The OWI can be used to realize a "End of Line" calibration via the analog output AOUT of the complete assembled sensor module.

Refer "ZMD31150 Functional Description" for a detailed description of the serial interfaces and communication protocols.

1.8 Safety Features, Watchdog and Error Detection

The ZMD31150 detects various possible errors. A detected error is signalized by changing in diagnostic mode (DM). In this case the analog output is set to LOW (minimum possible output value = lower diagnostic range – LDR) and the output registers of the digital serial interface are set to a significant error code. Power or

A watchdog oversees the continuous working of the CMC and the running measurement loop. The operation of the internal clock oscillator is verified continuously by oscillator fail detection.

A check of the sensor bridge for broken wires is done permanently by two comparators watching the input voltage of each input (sensor connection and short check). Additionally the common mode voltage of the sensor and sensor input short is watched permanently (sensor aging).

Different functions and blocks in digital part - like RAM-, ROM-, EEPROM- and register content - are watched continuously. Refer “ZMD31150 Functional Description” for a detailed description of safety features and methods of error messaging.

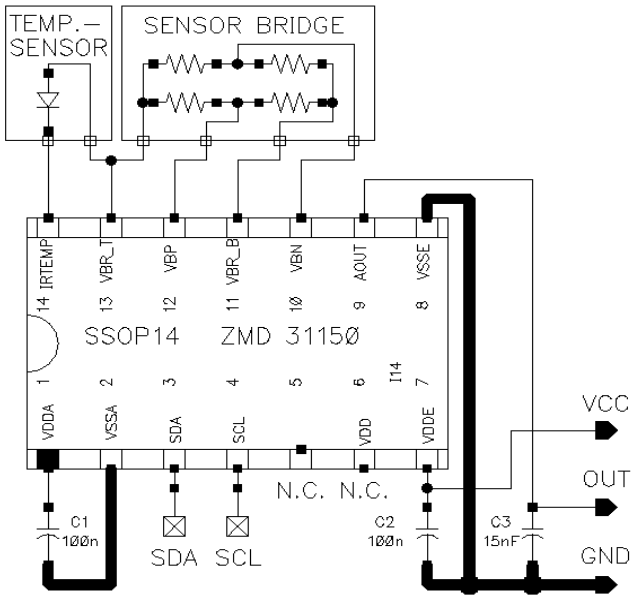
1.9 High Voltage, Reverse Polarity and Short Circuit Protection

The ZMD31150 is designed for 5V power supply operation.

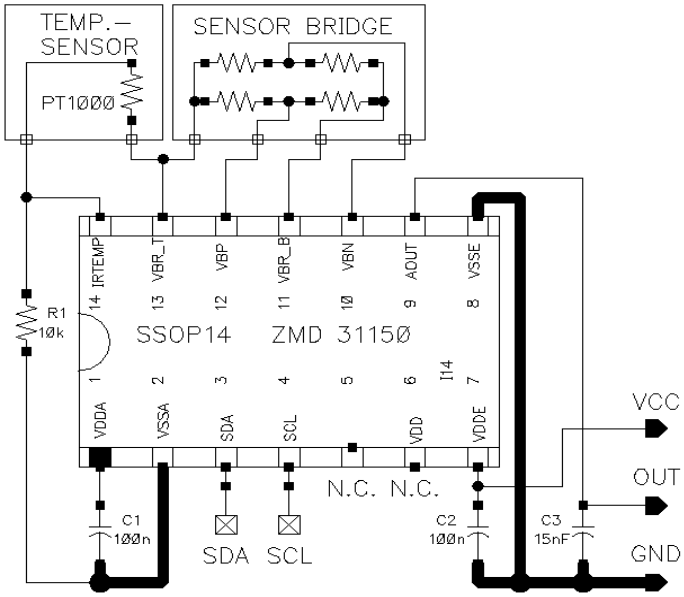
The ZMD31150 and the connected sensor is protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The analog output AOUT can be connected (short circuit, overvoltage and reverse) with all potentials in protection range under all potential conditions at the pins VDDE and VSSE.

All external components – explained in application circuit in chapter 2 – are required to guarantee these operation, the protection is no time limited. Refer “ZMD31150 High Voltage Protection Description” for a detailed description of protection cases and conditions.

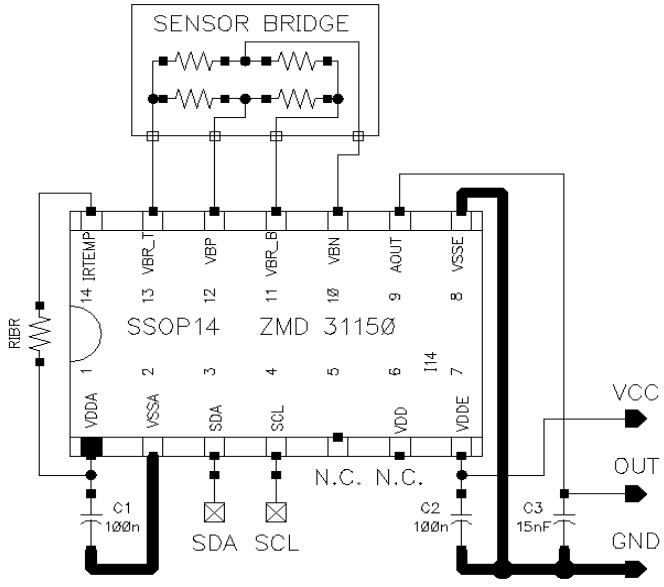
2. Application Circuit Example



Example 1:
Bridge in voltage mode, ext. diode temp sensor



Example 2:
Bridge in voltage mode, external thermistor



Example 3
Bridge in current mode, temp via bridge TC

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C1	C	100		470	nF
C2	C	100			nF
C3	C	4	15	30	nF
R1			10		kOhm
RIBR	R	refer 5.2.8			Ohm

Table 4: Application Circuit Parameters

The application circuits contain external components, which are needed for overvoltage, reverse polarity and short circuit protection.

3. ESD-Protection

All pins have an ESD Protection of >2000V. Additionally the pins VDDE, VSSE and AOUT have an ESD Protection of >4000V.

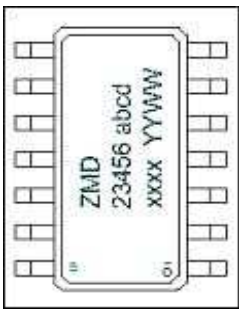
ESD Protection referred to the human body model is tested with devices in SSOP14 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

4. Pin Configuration, Latch-Up and Package

Pin	Name	Description	Remarks	Latch-Up related Application Circuit Restrictions and/or Remarks
9	AOUT	Analog output & one wire interface IO	IO	Trigger Current/Voltage: -100mA/33V
7	VDDE	Positive external supply voltage	Supply	Trigger Current/Voltage: -100mA/33V
6	VDD	Positive digital supply voltage	Analog IO	only capacitor to VSSA is allowed, otherwise no application access
8	VSSE	Negative external supply voltage	Ground	
4	SCL	I²C clock	Digital IN, pull-up	Trigger Current/Voltage to VDDA/VSSA: +/-100mA or 8/-4V
3	SDA	I²C data IO	Digital IO, pull-up	
2	VSSA	Negative analog supply voltage	Analog IO	
1	VDDA	Positive analog supply voltage	Analog IO	
13	VBR_T	Bridge top potential	Analog IO	
11	VBR_B	Bridge bottom potential	Analog IO	
14	IRTEMP	Current source resistor IO & temp. diode in	Analog IO	
12	VBP	Positive input sensor bridge	Analog IN	
10	VBN	Negative input sensor bridge	Analog IN	

Table 4: Pin Configuration and Latch-Up Conditions

The standard package of the ZMD31150 is a SSOP14 green package (5.3mm body width) with a lead-pitch 0.65mm:

Pin-Nr	Pin-Name		Pin-Name	Pin-Nr
8	VSSE		VDDE	7
9	AOUT		VDD	6
10	VBN		n.c.	5
11	VBR_B		SCL	4
12	VBP		SDA	3
13	VBR_T		VSSA	2
14	IRTEMP		VDDA	1

5. IC Characteristics

5.1 Absolute Maximum Ratings

In operation temperature range and without time limitations.

No.	Parameter	Symbol	min	typ	Max	Unit	Conditions
5.1.1	Supply Voltage [1]	$VDDE_{AMR}$	-18		33	V DC	to VSSE, refer chapter 2 for application circuits
5.1.2	Potential at Pin AOUT [1]	V_{OUT}	-18		33	V DC	related to VSSE
5.1.3	Analog Supply Voltage [1]	$VDDA_{AMR}$	-0.3		6.5	V DC	related to VSSA, V_{DDE}–V_{DDA} < 0.35V
5.1.4	Voltage at all analog and digital IO – Pins	V_{A_IO}, V_{D_IO}	-0.3		VDDA +0.3	V DC	related to VSSA
5.1.5	Storage temperature	T_{STG}	-55		150	°C	

5.2 Operating Conditions

All Voltages related to VSSA.

No.	Parameter	Symbol	min		Max	Unit	Conditions
5.2.1	Ambient temperature [2]	T_{AMB}	-40		150	°C	TQE [2]
5.2.2	Ambient temperature advanced performance *	T_{AMB_TQA}	-40		125	°C	TQA
5.2.3	Ambient temperature advanced performance *	T_{AMB_TQI}	-25		85	°C	TQI
5.2.4	Supply Voltage	VDDE	4.5		5.5	V DC	
	Bridge Voltage Mode						
5.2.5	Bridge Resistance *	R_{BR}	2.0		25.0	kΩ	
	Bridge Current Excitation						
5.2.7	Bridge Resistance *	R_{BR}			10	kΩ	notice I_{BR_MAX}
5.2.8	Resistor R_{IBR} *	R_{IBR}	0.07			R_{BR}	$I_{BR}=V_{DDA}/(16 \cdot R_{BR\_Ref})$
5.2.9	Maximum Bridge Current	I_{BR_MAX}			2	mA	
5.2.10	Maximum Bridge Top Voltage	V_{BR_TOP}			$\frac{15}{16} \cdot V_{DDA}$ – 0.3	V	

* no measurement in mass production, parameter is guarantied by design and/or quality observation
[1] refer "ZMD31150_HV_PROT_Rev*.PDF" for specification and detailed conditions
[2] notice temperature profile in "ZMD31150_DP_Rev*.PDF" for operation in temperature range 125 …150deg

5.2.11	TC Current Reference Resistor *	TK R_{IBR}		50		ppm/K	behaviour influences generated current

5.3 Electrical Parameters

All parameter values are valid on behalf on in chapter 5.2 specified operating conditions (special definitions excluded). All Voltages related to VSSA.

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.3.1 Supply Current and System Operation Conditions							
5.3.1.1	Supply current	I_{VDDE}			5.5	mA	without bridge and load current, $f_{CLK} \leq 3MHz$
5.3.1.2	Clock frequency	f_{CLK}	2 *	3	4 *	MHz	guaranteed adjustment range
5.3.2 AFE (refer chapter 1.3)							
5.3.2.1	Input Span	V_{IN_SP}	1		275	mV/V	analog gain: 420…2.8
5.3.2.2	Analog Offset Compensation Range		-300		300	% V_{IN_SP}	depends on gain adjust, refer 1.3.2
5.3.2.3	Parasitic differential input offset current *	I_{IN_OFF}	-2 -10		2 10	nA	T_{AMB_TQI}
5.3.2.4	Common mode input range	V_{IN_CM}	0.29		0.65	VDDA	depends on gain adjust, no XZC, refer 1.3.1
5.3.3 Temperature Measurement (refer chapter 1.4)							
5.3.3.1	External temperature diode channel gain	A_{TSED}	750		1800	ppm FS / mV	
5.3.3.2	External temperature diode bias current	I_{TSE}	6	10	20	µA	
5.3.3.3	External temperature diode input range *		0		1.2	V	
5.3.3.4	External temperature resistor channel gain	A_{TSER}	2700	6666 @GT1	8000	ppm FS / (mV/V)	
5.3.3.5	External temperature resistor input range *	V_{TSER}	0		270	mV/V	
5.3.3.7	Internal temperature diode sensitivity	ST_{TSI}	1650	3665 @GT1	4000	ppm FS /K	raw values – without conditioning
5.3.4 Sensor Connection Check							
5.3.4.1	Sensor connection loss		100			kΩ	detection threshold

* no measurement in mass production, parameter is guarantied by design and/or quality observation

5.3.4.2	Sensor input short				50	Ω	detection threshold

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.3.5 AD-Conversion							
5.3.5.1	A/D Resolution *	r_{ADC}	13		16	Bit	
5.3.5.2	DNL *	DNL_{ADC}			0.95	LSB	r_{ADC} =13Bit, f_{CLK}=3MHz, best fit, 2nd order, complete AFE
5.3.5.3	INL TQA *	INL_{ADC}			4	LSB	
5.3.5.4	INL TQE	INL_{ADC}			5	LSB	
5.3.6 DAC & Analog Output (Pin AOUT)							
5.3.6.1	D/A Resolution	r_{DAC}		12		Bit	analog output, 10-90%
5.3.6.2	Output current sink and source for VDDE=5V	$I_{SRC/SINK\_OUT}$			2.5 5	mA	Vout: 5-95%, R_{LOAD}>=2kΩ Vout: 10-90%, R_{LOAD}>=1kΩ
5.3.6.3	Short circuit current	I_{OUT_max}	-20		20	mA	to VSSE/VDDE
5.3.6.4	Addressable output signal range	V_{SR_OUT95} V_{SR_OUT90}	0.05 0.1		0.95 0.9	VDDE	@ R_{LOAD}>=2kΩ @ R_{LOAD}>=1kΩ
5.3.6.5	Output slew rate *	SR_{OUT}	0.1			V/µs	C_{LOAD} < 50nF
5.3.6.6	Output resistance in diagnostic mode	R_{OUT_DIA}			82	Ω	Diagnostic Range: <4/>96%, R_{LOAD}>=2kΩ <8/>92%, R_{LOAD}>=1kΩ
5.3.6.7	Load capacitance *	C_{LOAD}			150	nF	C3 + CL (refer chapter 2)
5.3.6.8	DNL	DNL_{OUT}	-1.5		1.5	LSB	
5.3.6.9	INL TQA *	INL_{OUT}	-5		5	LSB	best fit, r_{DAC} =12Bit
5.3.6.10	INL TQE	INL_{OUT}	-8		8	LSB	best fit, r_{DAC} =12Bit
5.3.6.11	Output Leakage current @ 150grd	I_{LEAK_OUT}			40	µA	in case of power or ground loss
5.3.7 System Response							
5.3.7.1	Startup time [1]	t_{STA}			5	ms	Power up to 1st conditioning result, fclk=3MHz, no ROM check
5.3.7.2	Response time (100% jump) *	t_{RESP}	256		512	µs	f_{CLK}=4MHz, 13Bit, 2nd order, refer chapter 0
5.3.7.3	Bandwidth *			5		kHz	comparable to analog SSCs

[1] Depends on resolution and configuration - start routine begins approximately 0.8ms after power on

* no measurement in mass production, parameter is guarantied by design and/or quality observation

5.3.7.4	Analog Output Noise Peak-to-Peak *	$V_{NOISE,PP}$			10	mV	shorted inputs, gain= bandwidth ≤ 10kHz
5.3.7.5	Analog Output Noise RMS *	$V_{NOISE,RMS}$			3	mV	shorted inputs, gain= bandwidth ≤ 10kHz
5.3.7.6	Ratiometricity Error	RE_{OUT_5}			1000	ppm	
5.3.7.7	Overall failure (deviation from ideal line including INL, gain, offset & temp errors)	F_{ALL} TQI F_{ALL} TQA F_{ALL} TQE		0.25 0.5 1.0		% FS	13Bit 2Step ADC, fclk<=3MHz, without sensor caused effects

5.4 Interface Characteristics & EEPROM

No.	Parameter	Symbol	min	typ	max	Unit	Conditions
5.4.1 I²C Interface							
5.4.1.1	Input-High-Level *	$V_{I2C\_IN\_H}$	0.8			VDDA	
5.4.1.2	Input-Low-Level *	$V_{I2C\_IN\_L}$			0.2	VDDA	
5.4.1.3	Output-Low-Level *	$V_{I2C\_OUT\_L}$			0.15	VDDA	Open Drain, I_{OL}<2mA
5.4.1.4	SDA load capacitance *	C_{SDA}			400	pF	
5.4.1.5	SCL clock frequency *	f_{SCL}			400	kHz	
5.4.1.6	Internal pullup resistor *	R_{I2C}	50		200	kΩ	
5.4.2 ZACwire™ One Wire Interface (OWI)							
5.4.2.1	Input-Low-Level *	$V_{OWI\_IN\_L}$			0.2	VDDA	
5.4.2.2	Input-High-Level *	$V_{OWI\_IN\_H}$	0.75			VDDA	
5.4.2.3	Output-Low-Level *	$V_{OWI\_OUT\_L}$			t.b.d.	VDDA	Open Drain, I_{OL}<?mA
5.4.2.4	Start Window *		96	175	455	ms	typ: @ fclk=3MHz
5.4.2.4	OWI						
5.4.3 EEPROM							
5.4.3.1	Ambient temperature EEPROM programming *	T_{AMB_EEP}	-40		150	°C	
5.4.3.2	EEPROM programming cycles *	n			100k 100		@write <= 85grd @write up to 150grd
5.4.3.3	EEPROM Data retention *	t_{RET_EEP}			15	a	100000h@<55grd & 27000h@<125grd & 3000h@<150grd [1]
5.4.3.4	EEPROM programming time *	t_{WRI_EEP}		12		ms	per written word, fclk=3MHz

* no measurement in mass production, parameter is guarantied by design and/or quality observation
[1] over lifetime and valid for the dice, notice additional package caused restrictions

6. Reliability

The ZMD31150 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

7. Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZM31150, ZMD can customize the circuit design by adding or removing certain functional blocks.

For it ZMD has a considerable library of sensor-dedicated circuitry blocks.

Thus ZMD can provide a custom solution quickly. Please contact ZMD for further information.

8. Related Documents

- ZMD31150 Feature Sheet - ZMD31150_FS_Rev_*.PDF
- ZMD31150 Functional Description - ZMD31150_FD_Rev_*.PDF
- ZMD31150 HighVoltage Protection Description - ZMD31150_HV_PROT_Rev_*.PDF
- ZMD31150 Application Kit Description - ZMD31150_APPLKIT_Rev_*.PDF
- ZMD31150 Development Status Report (including parts identification table)
- ZMD31150 Application Notes - ZMD31150_AN*.pdf

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Changes

V0.38: 5.3.6.6 referenced to load resistor
=> VDDA=4.5V => Vout(min)=4.5V*0.04=180mV => 0.18/(4.5-0.18)*2k = 83.3Ω
=> VDDA=5.5V => Vout(min)=5.5V*0.04=220mV => 0.22/(5.5-0.22)*2k = 83.3Ω

5.3.6.4 referenced to load resistor

5.3.6.2 valid for VDDE=5V (less supply gives less current for the same resistor!)

V0.40: 5.4.2 revised (refer ZMD31150_FD_Rev_0_40.pdf, chapter)