ZMD31030

Automotive Sensor Signal Conditioner with LIN Interface

Datasheet PRELIMINARY

1. General Description

The main building blocks are the following:

- Input multiplexer to select the input signal for the ADC, to select the internal or one of the external temperature sensors and to change the polarity of the pressure sensor bridge signal
- Chopper stabilized preamplifier for low noise and excellent drift behavior over temperature and age for the pressure sensor bridge signal
- Current sources for the external temperature sensors and for the internal temperature sensor
- Charge balancing ADC with ratiometric measurement of bridge signal and variable zero point for adapting to the sensor offset and with absolute measurement of temperature sensor signal, select by the input multiplexer
- LIN interface for calibration and testing and for communication in normal operation mode
- PWM output with low side switch (LSS) or high side switch (HSS)
- 3 Wire Interface for fast calibration and testing
- 16 bit calibration microcontroller (CMC) with ROM and EEPROM
- Reference sources, power-on-clear circuit, clock generator
- Voltage regulator to supply the analog and digital parts with an reduced voltage of 5V
- Low resistance switches to allow the reverse polarity at the output pin in PWM mode

The block diagram of the ASSP is shown in figure 1.

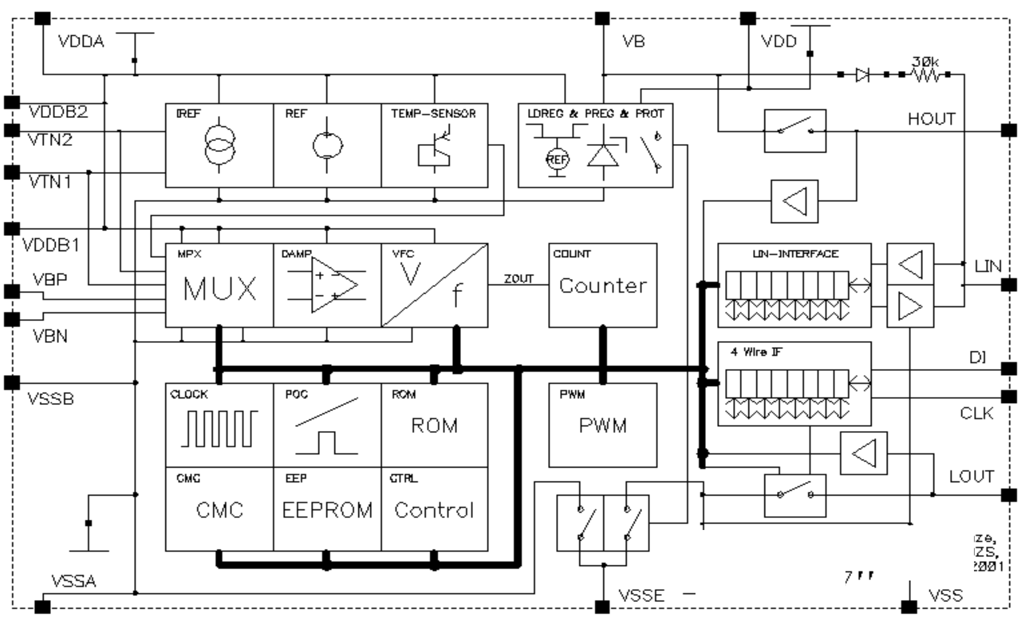

Fig. 1: Block diagram of the ZMD31030

3. Detailed Description

Analog signal conditioning

The measurement cycle is realized by the source selection of the multiplexer (MUX), controlled by the calibration micro controller (CMC). The MUX selects one of the following 4 input signals:

- Pressure signal bridge output voltage
- the first external temperature sensor supplied by an internal reference current source
- the second external temperature sensor supplied by an internal reference current source
- the internal temperature sensor, supplied by an internal reference current source.

The temperature sensors are realized as semiconductor diodes. Besides the input multiplexer allows to shorten the input wires of the ADC to realize the auto zero cycles and to change the polarity of the bridge inputs.

A complete measurement cycle consists of the following 4 parts:

- temperature auto zero measurement (one of the 3 temperature sensors)
- temperature measurement (one of the 3 temperature sensors)
- pressure auto zero measurement
- pressure measurement.

The pressure is ratiometric measured by using the internal stabilized power supply as ratiometric reference and the chopped full differential preamplifier to amplify the bridge signal.

The temperature sensor input can be changed cyclically between two different input signals. One of them is used for the calibration of the pressure sensor signal. The other one can be used to measure the temperature of an external medium. It is also possible to use the same sensor for the two measurements. The temperature is directly measured by the ADC by using a voltage reference for absolute measurement. The current source for the temperature measurement is a constant reference current source (non-ratiometric to VDDA). The current source for the bridge temperature sensor is only activated during the temperature measurement cycle to reduce the influence of leakage current during the pressure measurement.

The ADC is a first order charge balancing converter in full differential switched capacitor technique. It is inherently monotone and insensitive against short and long term instability of the clock frequency. The result of the AD conversion is a clock pulse stream corresponding to the following equation:

$$ZOUT = N * ((VIN / VREF) + OFF))$$

ZOUT: number of counts (result of the conversion)
N: number of clock pulses during one measurement
VIN: differential input voltage of ADC (VIN=VINP-VINN)
VREF: differential reference voltage (VREF=VREFP-VREFN)
OFF: offset value (OFF=$^1/_{16}$, $^1/_8$, $^1/_4$, $^1/_2$, controlled by the CMC)

With the OFF value a asymmetric sensor input signal can be shifted in the optimal input range of the ADC. The CMC controls the gain value of the preamplifier and the offset value of the ADC.
This values are stored in the EEPROM.

Digital parts (calibration micro controller (CMC), ROM, EEPROM, clock generator, power on clear circuit, control logic, ZOUT counter, PWM, 3 wire interface, LIN Interface)

The digital parts control the working modes of the ASSP and calculate the result of the measurement by use of the actual input data of pressure and temperature and the stored calibration coefficients.
The ASSP includes a 3 wire interface for test and calibration (further called command mode). A external master devices can read out the results of the measurements and store the values for modes, gain and offset, the calibration data, the LIN configuration data and the customer specific data.

During calibration cycles in command mode it is possible to read out the auto zero corrected values of the temperature and pressure measurements.
The calibration micro controller, the calibration procedure and the 3 wire calibration and test interface is described in detail in appendix A2.
The digital calculation done by the CMC compensate the following influences of the pressure output signal:
- Linear and quadratic pressure failure
- Linear and quadratic offset failure of the pressure signal over temperature
- Linear and quadratic sensor sensitivity failure over temperature.

Compensation of the medium temperature output signal (external diode):
- Linear and quadratic temperature failure

The operation modes of the ASSP are the High-Side-Switch mode (HSS, output signal is PWM), the Low-Side-Switch mode (LSS, output signal is PWM) and the LIN interface mode (LIN, output signal is a digital word).
In PWM modes the output signal is the calculated pressure value. The PWM minimal and maximal values can be adjusted and will be stored in the EEPROM.

In the LIN mode the communication occurs with the help of an LIN interface. A LIN slave is implemented in the ASSP. In the LIN normal operation mode the master device can read out the calibrated results of the pressure measurement and of the second external temperature sensor measurement. In command mode a master device can test and calibrate the ASSP in the real application circuit (i.e. the pressure sensor device in the automotive package) over the one wire LIN pin. The ID for the normal operation mode is stored in the EEPROM and can be changed in the command mode. The ID for the command mode is fixed by metal wires in the digital part of the ASSP. The LIN interface is described in detail in appendix A3 and correspond to the LIN Specification, Revision 1.2. from 17.11.2000 .

In the other application circuits (HSS and LSS) this command mode is also possible. The communication occurs over the pin LOUT (low side switch output pin) or the pin HOUT (high side switch output pin).
In LSS mode the active state of the data input and output is the same as in LIN mode (low active), in HSS this active state is inverted (high active) because of the open drain high side switch. The requirements for the output currents, output levels, input levels and slew rates of this communication are changed to the possibilities of the selected output mode specified for the normal operation mode as PWM output pin.
To switch the ASSP in this command mode a defined pulse cycle must be generated at the pin HOUT or LOUT during switch on the power supply. During this switched on time the ASSP output will be switched in tri state mode to allow the detection of the start pulses of this command mode.

High voltage protection (HV), short circuit protection and reverse polarity protection

The ASSP is directly supplied from the 12V power line.
An internal voltage regulator stabilized the internal supply voltage of approximately 5V.
To protect the ASSP against over voltage parallel voltage regulators, internal protection resistors and high voltage switches are integrated.
Reverse polarity protection is achieved with comparators, diodes and current limiting circuits.
These circuits allow a reverse polarity protection of the power supply pin and the used output pin without time limits.
The short circuit protection for the PWM output pin is realized by the control of the output level. When the output doesn't reach a specified value after a defined time period the ASSP recognize a shorted output and switch off the output switch.
The short protection for the LIN pin is realized by a current limited output switch.

Appendix A1 describes the behaviour of the ASSP in the several cases of protection.

4. Application Circuits

The figures 2, 3 & 4 show the circuit diagrams for applications of the ZMD31030.
The shown application circuits are design objectives and can be changed after the ASSP design process and after the measurement of the engineering samples.

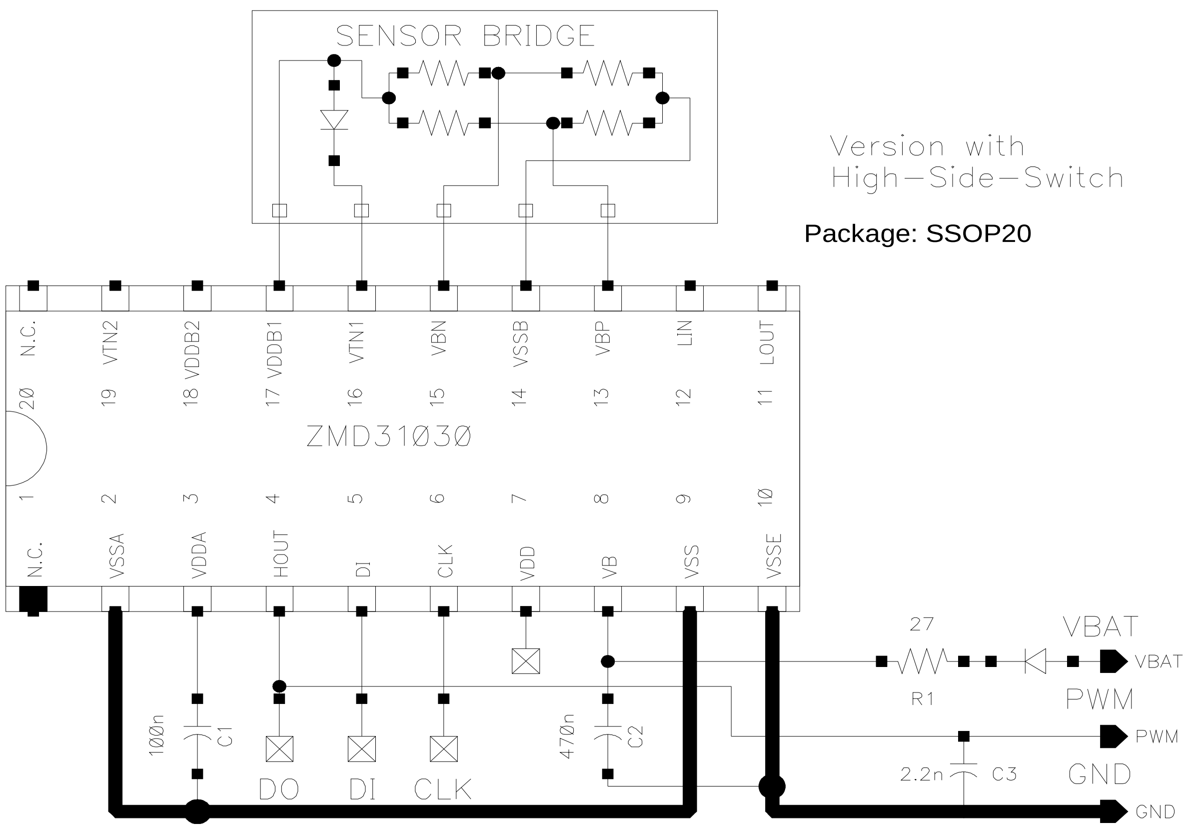

Fig. 2 : Circuit diagram for application “High-Side-Switch” of the ZMD31030

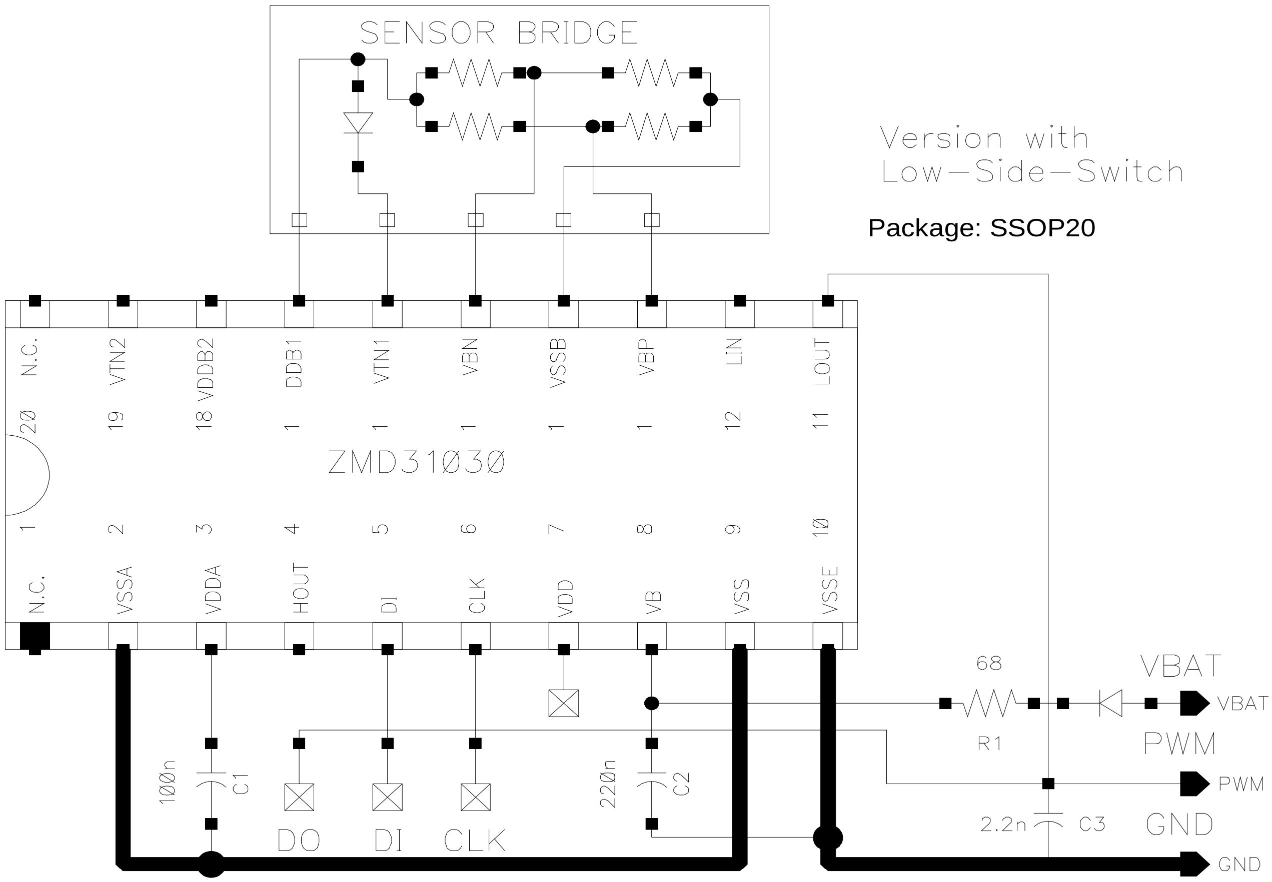

Fig. 3 : Circuit diagram for application "Low-Side-Switch" of the ZMD31030

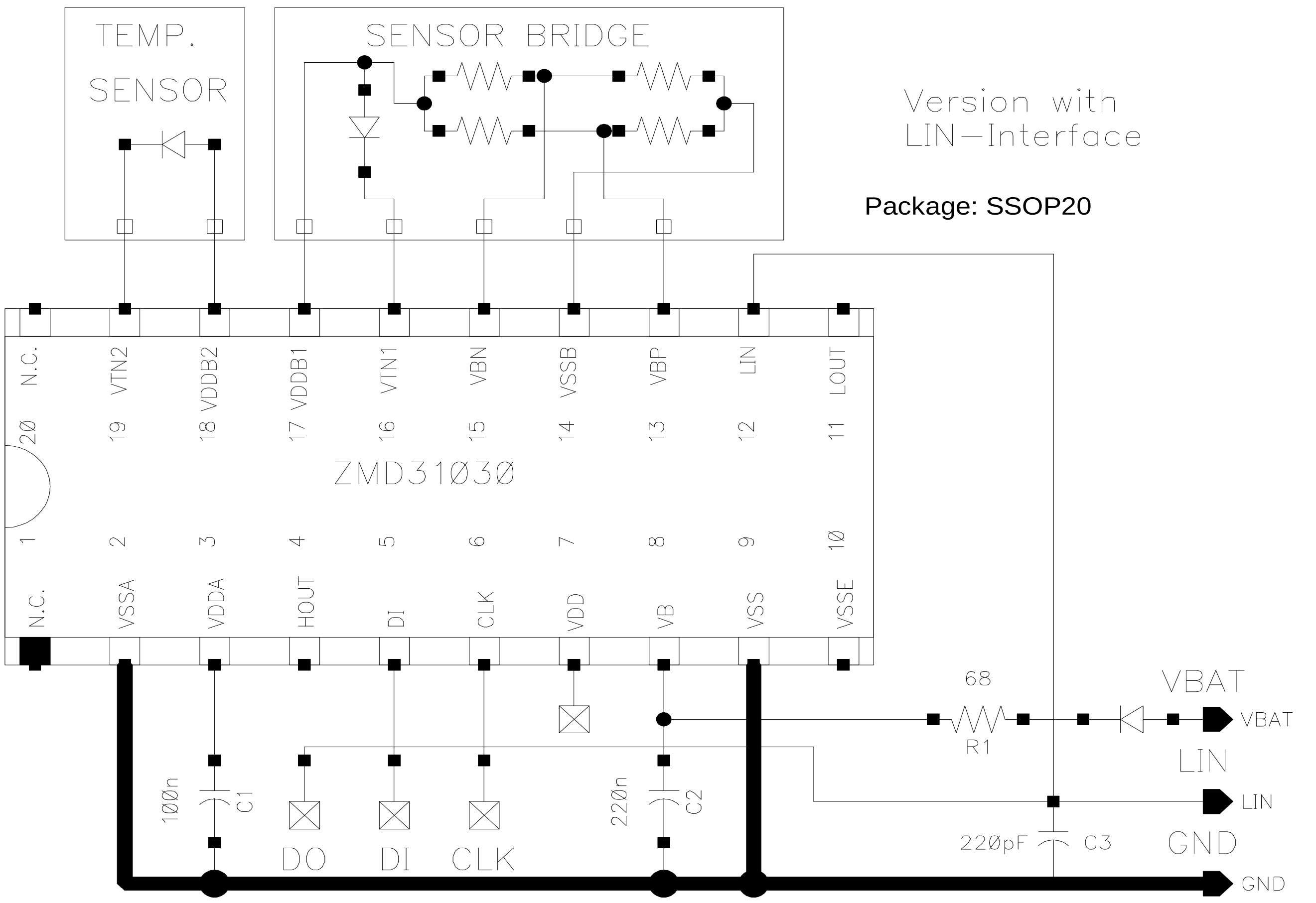

Fig. 4 : Circuit diagram for application “LIN-Interface” of the ASSP “ZMD31030”

4.1. Sizing of the external devices in the application circuits (Fig. 2, 3 & 4)

The final values will be fixed after testing of the prototype samples in the customer application board.

NR.	PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
4.1.1	Capacitance	C1	all modes		100		nF
4.1.2	Capacitance	C2	high side switch mode		470		nF
4.1.3	Capacitance	C2	low side switch mode		220		nF
4.1.4	Capacitance	C2	LIN mode		220		nF
4.1.5	Capacitance	C3	high side switch mode		2.2		nF
4.1.6	Capacitance	C3	low side switch mode		2.2		nF
4.1.7	Capacitance	C3	LIN mode		220		pF
4.1.8	Resistor	R1	high side switch mode		27		Ω
4.1.9	Resistor	R1	low side switch mode		68		Ω
4.1.10	Resistor	R1	LIN mode		68		Ω
4.1.11	Diode VBAT-> R1 (Standard-Si-Diode)						

The pin VDD allows the connection of an external capacitance in case of EMV problems.

5. Electrical Specification

HSS – High Side Switch Mode, LSS – Low Side Switch Mode, LIN – LIN-Interface-Mode,

Pin VSS and VSSA are shorted

5.1. Absolute Maximum Ratings

(all voltages referred to VSSA/ VSS)

NR.	PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
5.1.1	Supply voltage	V_B	HSS, LSS mode	-18	18	V
5.1.2	Supply voltage	V_{B_LIN}	LIN mode	-18	40	V
5.1.3	Voltage at pins LOUT, HOUT	V_{LOUT}, V_{HOUT}	to VSSE	-18	18	V
5.1.4	Voltage at pin LIN	V_{LIN}	to VSS	-18	18	V
5.1.5	Voltage at all digital inputs	V_{IND}, V_{OUTD}	to VSS	-0.3V	V_{DD}+ 0.3V	
5.1.6	Voltage at all analog inputs and outputs	V_{INA}, V_{OUTA}	to VSSA	-0.3V	V_{DDA}+ 0.3V	
5.1.7	Storage temperature	T_{STG}		-40	150	℃
5.1.8	Storage temperature	T_{STG}	t < 10h	-40	170	℃

5.2. Operating conditions

(all voltages referred to VSSA/ VSS)

NR.	PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
5.2.1	Supply voltage	V_B	to VSS / VSSE	8.2	12	16.5	V
5.2.2	Supply voltage	V_{B_PROG}	to VSS / VSSE	12.25	12.5	12.75	V
5.2.3	Supply voltage	V_{B_LIN}	to VSS	8	12	18	V
5.2.4	Ambient temperature	T_A		-40		125	℃
5.2.5	Ambient temperature EEPROM programming	T_{A_PROG}	3)	10		70	℃
5.2.6	Bridge Resistance	R_{BRIDGE}		2.4		10	kΩ

5.3. Electrical Parameters (all voltages referred to VSSA/ VSS, T_A=-40℃ ... +125℃)

NR.	PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
5.3.1 Supply Voltage/ Supply Current							
5.3.1.1	Supply Current	I_S	without I_{BRIDGE} + I_{PWM} + I_{LIN}			7.7	mA
5.3.2 PWM Output Parameters							
5.3.2.1	Output-H-Level HSS Pin HOUT	$V_{PWMHSSH}$	I_{SOURCE}=15mA, V_B≥8.8V to VSSE	4			V
5.3.2.2	Output-L-Level LSS Pin LOUT	$V_{PWMLSSL}$	I_{SINK}=12mA, to VSSE			0.5V	V
5.3.2.3	Leakage current Pin LOUT	I_{L_LOUT}	sink, H-Level			50	µA
5.3.2.4	Rise time HSS	t_{RISE}	V_{HOUT}= 0.5V-> 4V			15	µs
5.3.2.5	Fall time HSS	t_{FALL}	V_{LOUT}= 4V-> 0.5V			15	µs
5.3.2.6	PWM cycle time	t_{PER}		16	20	24	ms
5.3.2.7	Resolution	RES_{PWMFS}	PWM_{min_min} ... PWM_{max_max}	11			Bit
5.3.2.8	Resolution	RES_{PWMHS}	PWM_{min_max} ... PWM_{max_min}	10			Bit
5.3.2.9	Min. duty cycle	PWM_{min}	8 Bit	1		99	%
5.3.2.10	Max. duty cycle	PWM_{max}	8 Bit	1		99	%
5.3.3 Analog Inputs VBP, VBN (Pressure Sensor Bridge, PSB)							
Polarity of Input Voltage							
5.3.3.1	Input Voltage PSB Measurement	V_{INPSB}	BIT REVIN=0		VBP-VBN		
5.3.3.2	Input Voltage PSB Measurement	V_{INPSB}	BIT REVIN=1		VBN-VBP		
Input Mode A							
5.3.3.3	Span	V_{PSB_A}		0.09			VDDA
5.3.3.4	Mode A1 Input Range	V_{PSB_A1}	OFF=1/16	-0.005625		0.084375	VDDA
5.3.3.5	Mode A2 Input Range	V_{PSB_A2}	OFF=1/8	-0.01125		0.07875	VDDA
5.3.3.6	Mode A3 Input Range	V_{PSB_A3}	OFF=1/4	-0.0225		0.0675	VDDA
5.3.3.7	Mode A4 Input Range	V_{PSB_A4}	OFF=1/2	-0.045		0.045	VDDA
5.3.3.8	Sensitivity	S_{PSB_A}	V_{DDA}=5V		128		µV/LSB
Input Mode B							
5.3.3.9	Span	V_{PSB_B}		0.06			VDDA
5.3.3.10	Mode B1 Input Range	V_{PSB_B1}	OFF=1/16	-0.00375		0.05625	VDDA
5.3.3.11	Mode B2 Input Range	V_{PSB_B2}	OFF=1/8	-0.0075		0.0525	VDDA
5.3.3.12	Mode B3 Input Range	V_{PSB_B3}	OFF=1/4	-0.015		0.045	VDDA
5.3.3.13	Mode B4 Input Range	V_{PSB_B4}	OFF=1/2	-0.03		0.03	VDDA
5.3.3.14	Sensitivity	S_{PSB_B}	V_{DDA}=5V		85		µV/LSB

NR.	PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Mode C							
5.3.3.15	Span	V_{PSB_C}		0.036			VDDA
5.3.3.16	Mode C1 Input Range	V_{PSB_C1}	OFF=1/16	-0.002		0.034	VDDA
5.3.3.17	Mode C2 Input Range	V_{PSB_C2}	OFF=1/8	-0.004		0.032	VDDA
5.3.3.18	Mode C3 Input Range	V_{PSB_C3}	OFF=1/4	-0.009		0.027	VDDA
5.3.3.19	Mode C4 Input Range	V_{PSB_C4}	OFF=1/2	-0.018		0.018	VDDA
5.3.3.20	Sensitivity	S_{PSB_C}	V_{DDA}=5V		50		µV/LSB
Input Mode D							
5.3.3.21	Span	V_{PSB_D}		0.02			VDDA
5.3.3.22	Mode D1 Input Range	V_{PSB_D1}	OFF=1/16	-0.001		0.019	VDDA
5.3.3.23	Mode D2 Input Range	V_{PSB_D2}	OFF=1/8	-0.002		0.018	VDDA
5.3.3.24	Mode D3 Input Range	V_{PSB_D3}	OFF=1/4	-0.005		0.015	VDDA
5.3.3.25	Mode D4 Input Range	V_{PSB_D4}	OFF=1/2	-0.01		0.01	VDDA
5.3.3.26	Sensitivity	S_{PSB_D}	V_{DDA}=5V		29		µV/LSB
All Input Modes							
5.3.3.27	Input Leakage Current	I_{INL}	differential, 1)	-40		40	nA
5.3.4 Analog Inputs VTN1, VTN2 (External Temperature Sensors, TSE1 and TSE2)							
5.3.4.1	Input Voltage Range	V_{IN_TSE}	to VDDB1_2	-810		-210	mV
5.3.4.2	Sensitivity	S_{TSE}			0.85		mV/ LSB
5.3.5 Internal Temperature Sensor (TSI)							
5.3.5.1	Sensitivity (to temperature)	S_{TTSI}		1.9	2.1	2.3	mV/K
5.3.5.2	Sensitivity	S_{TSI}			0.85		mV/ LSB
5.3.6 Current Source for External Temperature Sensor							
5.3.6.1	Output Current	I_{TSE}	sink	30	40	50	µA
5.3.6.2	Temperature Coefficient	TC_{ITSE}	1)	-1000		1000	ppm/K
5.3.7 Analog to Digital Conversion							
5.3.7.1	Resolution Pressure Signal Bridge	RES_{PSB}	1)	4096			Counts
5.3.7.2	Differential Nonlinearity	DNL_{PSB}	1)	-0.5		0.5	Bit
5.3.7.3	Integral Nonlinearity	INL_{PSB}	referred to best-fit straight line, 1)	-0.5		0.5	Bit
5.3.7.4	Resolution Temperature Sensor	RES_{TS}	1)	1024			Counts
5.3.7.5	Differential Nonlinearity (TS)	DNL_{TS}	1)	-0.5		0.5	Bit
5.3.7.6	Integral Nonlinearity (TS)	INL_{TS}	referred to best-fit straight line, 1)	-0.5		0.5	Bit

NR.	PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
5.3.8 Serial 3 wire Interface (all voltages referred to VSS)							
5.3.8.1	Input High Level	V_{IH}	Pins DI and CLK	0.7		1	VDD
5.3.8.2	Input Low Level	V_{IL}	Pins DI and CLK	0		0.3	VDD
5.3.8.3	Output Low Level DOUT=LIN	V_{OL_LIN}	I_sink = 10mA			1.2	V
5.3.8.4	Output Low Level DOUT=LOUT	V_{OL_LOUT}	I_sink = 10mA			0.5	V
5.3.8.5	Output High Level DOUT=HOUT	V_{OH_HOUT}	I_source = 10mA	4			V
5.3.8.6	Pull down Current	I_{OL}	I_sink, Pins DI and CLK	5		20	µA
5.3.8.7	Load Capacitance DOUT (HOUT, LOUT or LIN)	C_{L_DOUT}				2.5	nF
5.3.8.8	Clock Frequency CLK	f_{CLK}	C_{L_DOUT} = 2.5nF			400	kHz
5.3.8.9	Clock Frequency CLK	f_{CLK}	C_{L_DOUT} = 220pF			2000	kHz
5.3.8.10	Programming Voltage	V_{VPP}			13		V
5.3.8.11	Duration Programming Impulse	t_{VPP}	generated internally		10		ms
5.3.9 LIN Interface (all voltages referred to VSS, see Appendix A3)							
5.3.9.1	Output low voltage level	V_{LIN_OL}	I_{SINK} = 40mA			1.2	V
5.3.9.2	Output current	I_{LIN_L}	sink, driver on	40		120	mA
5.3.9.3	Output current	I_{LIN_H}	source, driver off			1.1	VBAT/ R_{LIN}
5.3.9.4	Pull up resistance	R_{SLAVE}	with serial diode	20	30	47	kΩ
5.3.9.5	Output current (Over voltage at LIN)	$I_{LIN\_H\_OV}$	sink, driver off, VLIN ≥ VBAT, 8V ≤ VBAT ≤ 18V			20	µA
5.3.9.6	Output current (GND lost)	I_{LIN_LOSTGL}	driver off, -12V ≤ VLIN ≤ 0V	-1		1	mA
5.3.9.7	Output current (GND lost, not specified in LIN spec. Rev. 1.2)	I_{LIN_LOSTGH}	driver off, -18V≤VLIN≤ -12V		t.b.d.		
5.3.9.8	Output current (VBAT lost)	I_{LIN_LOSTBH}	driver off, excluded pull-up, -18V≤VLIN≤ 18V	-40		40	µA
5.3.9.9	Input low voltage level (dominant state)	I_{LIN_IL}	driver off	-8V		0.4 * VBAT	
5.3.9.10	Input high voltage level (recessive state)	I_{LIN_IH}	driver off	0.6 * VBAT		18V	
5.3.9.11	Slew Rate (Rising and falling edges)	$SR_{LIN\_}$	transmit and receive	1	2	3	V/µs
5.3.9.12	Capacitance of slave node	C_{L_DOUT}			220	250	pF

NR.	PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
5.3.10 Total System							
5.3.10.1	Startup time	t_{STUP}	Power up to first output value			40	ms
5.3.10.2	Response Time	t_R				11	ms
5.3.10.3	Cycle Time	t_C	Complete cycle			10	ms
5.3.10.4	Nonlinearity	NL	referred to best-fit straight line 2)	-500		+500	ppm
5.3.10.5	Temperature dependency PSB Measurement	t_{CPSBM}				20	ppm/K
5.3.10.6	Temperature dependency TS Measurement	t_{CTSM}				100	ppm/K

1) No measurement in mass production, parameter is guarantied by design or will be tested within the product qualification.

2) Analog Signal Conditioning and Analog Digital Conversion for Measurement of the Pressure Sensor Bridge

3) The increase of the maximum temperature for EEPROM programming is possible after successfully qualification measurements under extended ambient temperature.

6. I/O Pin Definition and Description (see Fig. 5)

TIF - test interface - 3 wire interface for calibration and testing

PIN DIE	PIN SSOP20	PIN CDIP28	Name	Description	Remarks
	1		N.C.	not connected	
1	2	8	VSSA	negative internal supply voltage analog part	
2	3	12	VDDA	positive internal supply voltage analog part	
3	4	13	HOUT	PWM output high side switch mode (HSS), TIF data out and LIN data out for testing	CMOS, HV output
4	5	14	DI	digital input TIF data in	CMOS, internal pull-down
5	6	15	CLK	digital input TIF clock	CMOS, internal pull-down
6	7	16	VDD	positive internal supply voltage digital part	only connected in case of EMC problems
7	8	17	VB	positive supply voltage	CMOS, HV input/ output
8	9	18	VSS	negative internal supply voltage digital part, negative supply voltage in LIN mode	
9	10	21	VSSE	negative supply voltage in HSS mode and LSS mode	CMOS, HV input/ output
10	11	22	LOUT	PWM output low side switch mode (LSS), TIF data out and LIN data out for testing	CMOS, HV output
11	12	25	LIN	LIN input/ output, TIF data out for testing	CMOS, HV input/ output
12	13	26	VBP	positive input sensor bridge	CMOS, analog input
13	14	27	VSSB	negative supply voltage sensor bridge	CMOS, analog output
14	15	28	VBN	negative input sensor bridge	CMOS, analog input
15	16	1	VTN1	negative input temp. sensor 1	CMOS, analog input
16	17	2	VDDB1	positive supply voltage sensor bridge	CMOS, analog output, internal conn. to VDDB2
17	18	3	VDDB2	positive supply voltage sensor bridge	CMOS, analog output, internal conn. to VDDB1
18	19	7	VTN2	negative input temp. sensor 2	CMOS, analog input
	20	4	N.C.	not connected	
		5	N.C.	not connected	
		6	N.C.	not connected	
		9	N.C.	not connected	
		10	N.C.	not connected	
		11	N.C.	not connected	
		19	N.C.	not connected	
		20	N.C.	not connected	
		23	N.C.	not connected	
		24	N.C.	not connected	

7. Package

The ZMD31030 is supplied as die (size of bond pads is 90µm*90µm).
Engineering samples are supplied in SSOP20 (209mil) or in CDIP28 (600mil).

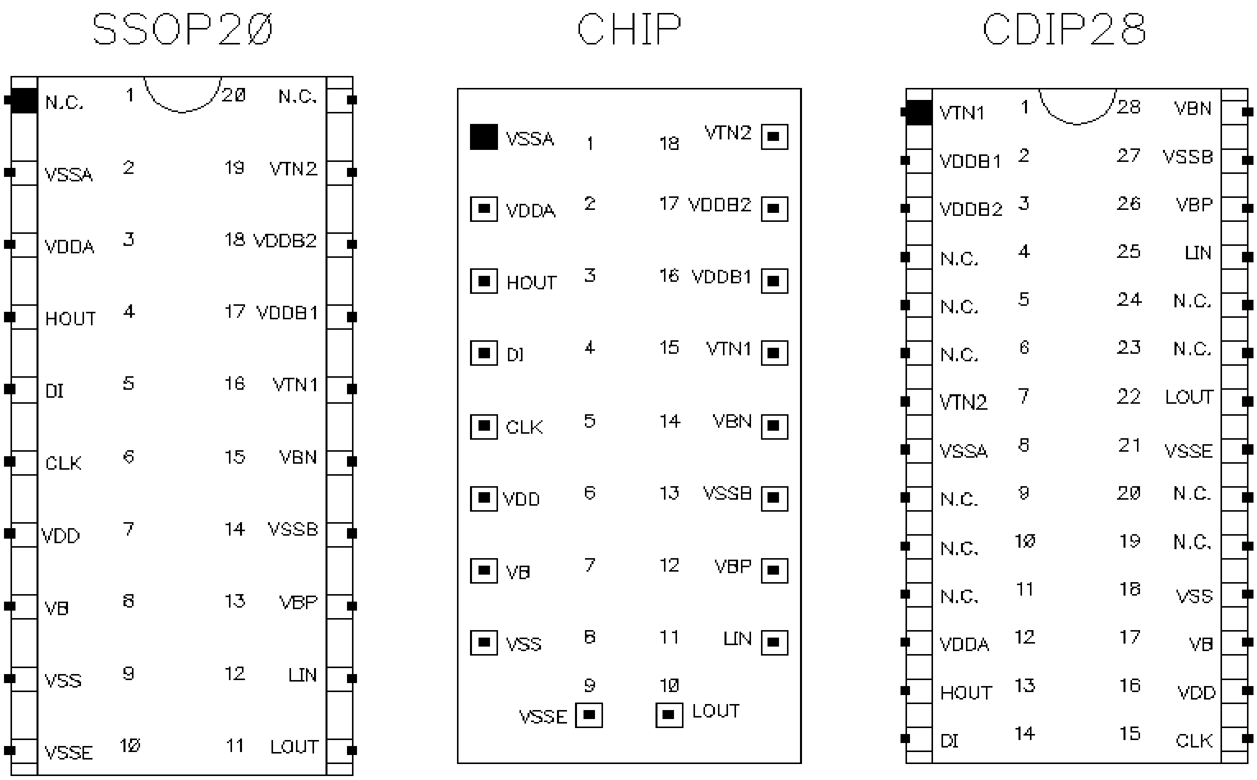

Fig. 5: Packages of the ZMD31030 with the Pin Definitions

8. Test

Parameters given in this specification are design objectives. Final parameters which will be tested during series production will be specified after investigations in the engineering samples. The resulting data sheet includes all parameters which will be tested by ZMD. The test program is based on this data sheet. The fulfillment of the test specification is obligatory to deliver and obligates to purchase.

9. ESD/Latch-Up-Protection

All Pins have an ESD Protection of >2000V.
ESD Protection referred to the human body model is tested with devices in SSOP20 packages during product qualification.

The Latch-up protection of the ZMD31030 is tested under the conditions shown in the following table with devices in SSOP20 packages during product qualification.

Pin-Nr. DIE	Pin–Nr. SSOP20	Name	Trigger current positive [mA]	Trigger current negative [mA]	Trigger voltage positive [V]	Trigger voltage negative [V]	Remarks
1	2	VSSA	100	100			Ground
2	3	VDDA			8.25		internal Power Supply, Overvoltage Test with 1.5*$VDDA_{MAX}$
3	4	HOUT		100	27		
4	5	DI		100	9		
5	6	CLK		100	9		
6	7	VDD			8.25		internal Power Supply, Overvoltage Test with 1.5*VDD_{MAX}
7	8	VB		100	27		Power Supply, Overvoltage Test with 1.5*VB_{MAX}
8	9	VSS					Ground
9	10	VSSE					Ground
10	11	LOUT		100	27		
11	12	LIN		100	27		
12	13	VBP			9	4	
13	14	VSSB					internal Ground
14	15	VBN			9	4	
15	16	VTN1			9	4	
16	17	VDDB1			8.25		internal Power Supply, Overvoltage Test with 1.5*$VDDA_{MAX}$
17	18	VDDB2			8.25		internal Power Supply, Overvoltage Test with 1.5*$VDDA_{MAX}$
18	19	VTN2			9	4	

10. Reliability

The ZMD31030 is produced without burn–in procedure.

11. Related Documents (available on request)

A1: Description of the high voltage protection circuit

A2: Functional Description

A3: Description of the LIN interface

A4: Layout and pad coordinates

12. Notes

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