ZMD31010

RBic$_{Lite}$™ Low-Cost Sensor Signal Conditioner

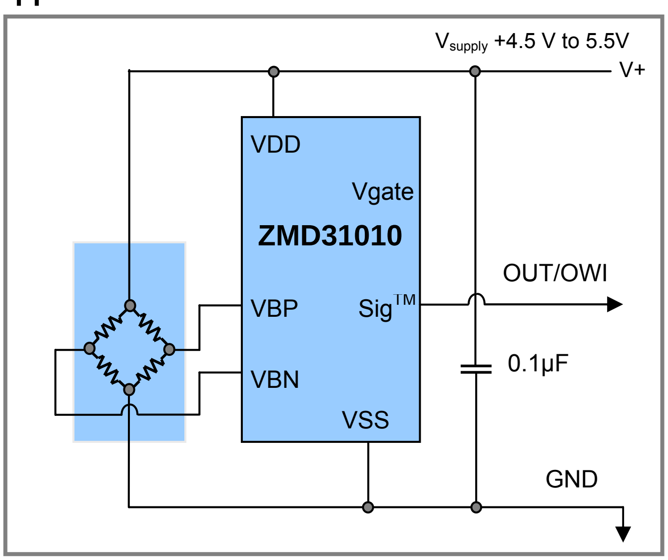
Datasheet

Features

- Digital compensation of sensor offset, sensitivity, temperature drift and non-linearity
- Accommodates differential sensor signal spans from 1.2mV/V to 60mV/V
- ZACwire™ one-wire interface.
- Internal temperature compensation and detection via bandgap PTAT*
- Optional sequential output of both temperature and bridge readings on ZACwire™ digital output
- Output options: rail-to-rail analog output voltage, absolute analog voltage, digital one-wire interface
- Supply voltage 2.7 to 5.5V, with external JFET 5.5V to 30V
- Current consumption, depending on adjusted sample rate: 0.25mA to 1mA
- Wide operational temperature: –50 to +150°C
- Fast response time 1ms (typical)
- High voltage protection up to 30V with external JFET
- Chopper-stabilized true differential ADC
- Buffered and chopper-stabilized output DAC

* Proportional to absolute temperature

Application Circuit



Typical RBic $_{Lite}$™ Application Circuit

Benefits

- No external trimming components required
- PC-controlled configuration and calibration via one-wire interface – simple, low cost
- High accuracy (±0.1% FSO @ -25 to 85°C; ±0.25% FSO @ -50 to 150°C)
- Single pass calibration – quick and precise
- Suitable for battery-powered applications
- Small SOP8 package

Brief Description

The RBic$_{Lite}$™ is a CMOS integrated circuit, which enables easy and precise calibration of resistive bridge sensors via EEPROM. When mated to a resistive bridge sensor, it will digitally correct offset and gain with the option to correct offset and gain coefficients and linearity over temperature. A second order compensation can be enabled for temperature coefficients of gain and offset or bridge linearity. RBic$_{Lite}$™ communicates via ZMD's ZACwire™ serial interface to the host computer and is easily mass calibrated in a Windows® environment. Once cali-brated, the output Sig™ pin can provide selectable 0 to 1V, rail-to-rail ratiometric analog output, or digital serial output of bridge data with optional temperature data.

- **Development Kit available**
- **Multi-Unit Calibrator Kit available**
- **Support for industrial mass calibration available**
- **Quick circuit customization possible for large production volumes**

ZMD31010

RBic$_{Lite}$™ Low-Cost Sensor Signal Conditioner

Datasheet

CONTENTS

ZMD31010

$RBic_{Lite}$™ Low-Cost Sensor Signal Conditioner

Datasheet

1 IC Characteristics

1.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply Voltage	V_{DD}	-0.3		6.0	V
Voltages at Analog I/O – In Pin	V_{INA}	-0.3		V_{DD}+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}	-0.3		V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	-50		150	°C
Storage Temperature Range	T_{STG}<10h	-50		170	°C

1.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Supply Voltage to Gnd	V_{DD}	2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	V_{SUPP}	5.5	7	30	V
Common Mode Voltage	V_{CM}	1		V_{DDA}-1.3	V
Ambient Temperature Range [1&2]	T_{AMB}	-50		150	°C
External Capacitance between V_{DD} and Gnd	C_{VDD}	100	220	470	nF
Output Load Resistance to V_{SS} or V_{DD} [3]	$R_{L,OUT}$	2.5	10		kΩ
Output Load Capacitance[4]	$C_{L,OUT}$		10	15	nF
Bridge Resistance [5]	R_{BR}	0.2		100	kΩ
Power ON Rise Time	t_{PON}			100	ms

[1] *Note that the maximum calibration temperature is 85°C.*

[2] *If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.*

[3] *When using the output for digital calibration, no pull down resistor is allowed.*

[4] *Using the output for digital calibration, $C_{L,OUT}$ is limited by the maximum rise time $T_{ZAC,rise}$.*

[5] *Note: Minimum bridge resistance is only a factor if using the Bsink feature. The nominal R_{DS}(ON) of the Bsink transistor is 10Ω when operating at VDD=5V, and 15Ω when operating at V_{DD}=3.0V. This does give rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.*

1.3 Electrical Parameters

See important footnotes at the end of the following table.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE / REGULATION						
Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Supply Current (varies with update rate and output mode)	I_{DD}	At minimum update rate.		250		µA
		At maximum update rate.		1000		µA
Temperature Coefficient – Regulator (worst case)	TC_{REG}	Temperature -10°C to 120°C			35	ppm/K*
		Temperature <-10°C and>120°C			100	ppm/K*
Power Supply Rejection Ratio	PSRR	DC < 100 Hz (JFET regulation loop using mmbf4392 and 0.1µF decoupling cap)	60			dB*
Power Supply Rejection Ratio	PSRR	AC < 100 kHz (JFET regulation loop using mmbf4392 and 0.1µF decoupling cap)	45			dB*
Power-On Reset Level	POR		1.4		2.6	V
ANALOG FRONT END (AFE)						
Leakage Current Pin VBP,VBN	I_{IN_LEAK}				±10	nA
ANALOG TO DIGITAL CONVERTER (ADC)						
Resolution	r_{ADC}			14		Bits
Integral Nonlinearity[1] (INL)	INL_{ADC}	Based on ideal slope	-4		+4	LSB
Differential Nonlinearity (DNL)	DNL_{ADC}		-1		+1	LSB*
Response Time	$T_{RES,ADC}$	Varies with update rate. Value given at fastest rate.		1		ms
ANALOG OUTPUT PARAMETERS (DAC + BUFFER)						
Max. Output Current	I_{OUT}	Max current maintaining accuracy	2.2			mA
Resolution	r_{OUT}	Referenced to V_{DD}			11	Bit
Absolute Error	E_{ABS}	DAC input to output	-10		+10	mV
Differential Nonlinearity	DNL	No missing codes	-0.9		+1.5	LSB_{11Bit}*
Upper Output Voltage Limit	V_{OUT}	R_L =2.5kΩ	95%			V_{DD}
Lower Output Voltage Limit	V_{OUT}				2.5	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		ZACwire™ Serial Interface*				
ZACwire™ Line Resistance	$R_{ZAC,line}$	See important limitations in footnote 2 below.			3.9	kΩ
ZACwire™ Load Capacitance	$C_{ZAC,load}$	See important limitations in footnote 2 below.	0	1	15	nF
ZACwire™ Rise Time	$T_{ZAC,rise}$				5	µs
Voltage Level Low	$V_{ZAC,low}$			0	0.2	V_{DD}
Voltage Level High	$V_{ZAC,low}$		0.8	1		V_{DD}
		TOTAL SYSTEM				
Start-Up-Time	t_{STA}	Power-up to output			10	ms
Response Time	t_{RESP}	Update_rate=1kHz (1ms)		1	2	ms
Sampling Rate	f_S	Update_rate=1kHz (1ms)		1000		Hz
Supply Current	I_{DD}	Update_rate=1kHz (1ms)		1		mA
Overall Linearity Error	E_{LIND}	Bridge input to output – Digital		0.025	0.04	%
Overall Linearity Error	E_{LINA}	Bridge input to output – Analog		0.1	0.2	%
Overall Ratiometricity Error	RE_{out}	Not using Bsink feature			0.035	%
Overall Accuracy – Digital (only IC, without sensor bridge)[3]	AC_{outD}	-25°C to 85°C -50°C to 150°C			±0.1% ±0.25%	%FSO %FSO
Overall Accuracy – Analog [3, 4] (only IC, without sensor bridge)	AC_{outA}	-25°C to 85°C -40°C to 125°C -50°C to 150°C			±0.25% ±0.35% ±0.5%	%FSO %FSO

** The parameters with an * under "Units" are tested by design.*

[1] Note: This is ± 4 LSBs to the 14-bit A-to-D conversion. This implies absolute accuracy to 12-bits on the A-to-D result. Non-linearity is typically better at temperatures less than 125°C.

[2] The rise time must be $T_{ZAC,rise} = 2\, R_{ZAC,line} * C_{ZACload} \leq 5\mu s$. If using a pull up resistor instead of a line resistor, it must meet this specification.

[3] A random additional noise in a very small temperature range (<2°C) or small range of the supply voltage can appear. For more details, refer to ZMD31010_RBic_Lite_Errata_RevB_prod.pdf .

[4] Not included is the quantization noise of the DAC. The 11-bit DAC has a quantization noise of ± ½ LSB = 1.22mV (5V VDD) = 0.025%.

1.4 Analog Inputs versus Output Resolution

RBic $_{Lite}$™ incorporates an extended 14-bit charge-balanced ADC which allows for a single gain setting on the pre-amplifier to handle bridge sensitivities from 1.2 to 36mV/V while maintaining 8 to 12 bits of output resolution (default analog gain 24). The tables below illustrate the minimum resolution achievable for a variety of bridge sensitivities. The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Analog Gain 6				
Input Span (mV/V)			Allowed Offset (+/- % of Span)[1]	Minimum Guaranteed Resolution (Bits)
Min	Typ	Max		
57.3	80.0	105.8	38%	13.3
50.6	70.0	92.6	53%	13.1
43.4	60.0	79.4	73%	12.9
36.1	50.0	66.1	101%	12.6
28.9.5	40.0	52.9	142%	12.3
21.7	30.0	39.7	212%	11.9

Analog Gain 12				
Input Span (mV/V)			Allowed Offset (+/- % of Span)[1]	Minimum Guaranteed Resolution (Bits)
Min	Typ	Max		
43.3	60.0	79.3	3%	13.0
36.1	50.0	66.1	17%	12.7
25.3	35.0	46.3	53%	12.2
18.0	25.0	33.0	101%	11.7
14.5	20.0	26.45	142%	11.4
7.2	10.0	13.22	351%	10.4
3.6	5.0	6.6	767%	9.4

[1]*In addition to Tco,Tcg*

Analog Gain 24				
Input Span (mV/V)			Allowed Offset (+/- % of Span)[1]	Minimum Guaranteed Resolution (Bits)
Min	Typ	Max		
16	25.0	36	25%	12.6
12.8	20.0	28.8	50%	12
6.4	10.0	14.4	150%	11
3.2	5.0	7.2	400%	10
1.6	2.5	3.6	900%	9
0.8	1.2	1.7	2000%	8

[1]*In addition to Tco,Tcg*

Analog Gain = 48				
Input Span (mV/V)			Allowed Offset (+/- % of Span)[1]	Minimum Guaranteed Resolution (Bits)
Min	Typ	Max		
10.8	15.0	19.8	3%	13
7.2	10.0	13.2	35%	12.4
4.3	6.0	7.9	100%	11.7
2.9	4.0	5.3	190%	11.1
1.8	2.5	3.3	350%	10.4
1.0	1.4	1.85	675%	9.6
0.72	1.0	1.32	975%	9.1

[1]*In addition to Tco,Tcg*

2 Circuit Description

2.1 Signal Flow and Block Diagram

The RBic$_{Lite}$™ series of resistive bridge sensor interface ICs were specifically designed as a cost-effective solution for sensing in building automation, industrial, office automation and white goods applications.

The RBic$_{Lite}$™ employs ZMD's high precision bandgap with proportional-to-absolute-temperature (PTAT) output; low-power 14-bit analog-to-digital converter (ADC, A2D, A-to-D); and on-chip DSP core with EEPROM to precisely calibrate the bridge output signal.

Three selectable outputs, two analog and one digital, offer the ultimate in versatility across many applications.

The RBic$_{Lite}$™ rail-to-rail ratiometric analog output V_{out} signal (0 to 5V V_{out} @ V_{DD}=5V) suits most building automation and automotive requirements.

Typical office automation and white goods applications require the 0~1V_{out} signal, which in the RBic$_{Lite}$™ is referenced to the internal bandgap.

Direct interfacing to µP controllers is facilitated via ZMD's single-wire serial ZACwire™ digital interface.

RBic$_{Lite}$™ is capable of running in high-voltage (5.5-30V) systems when combined with an external JFET.

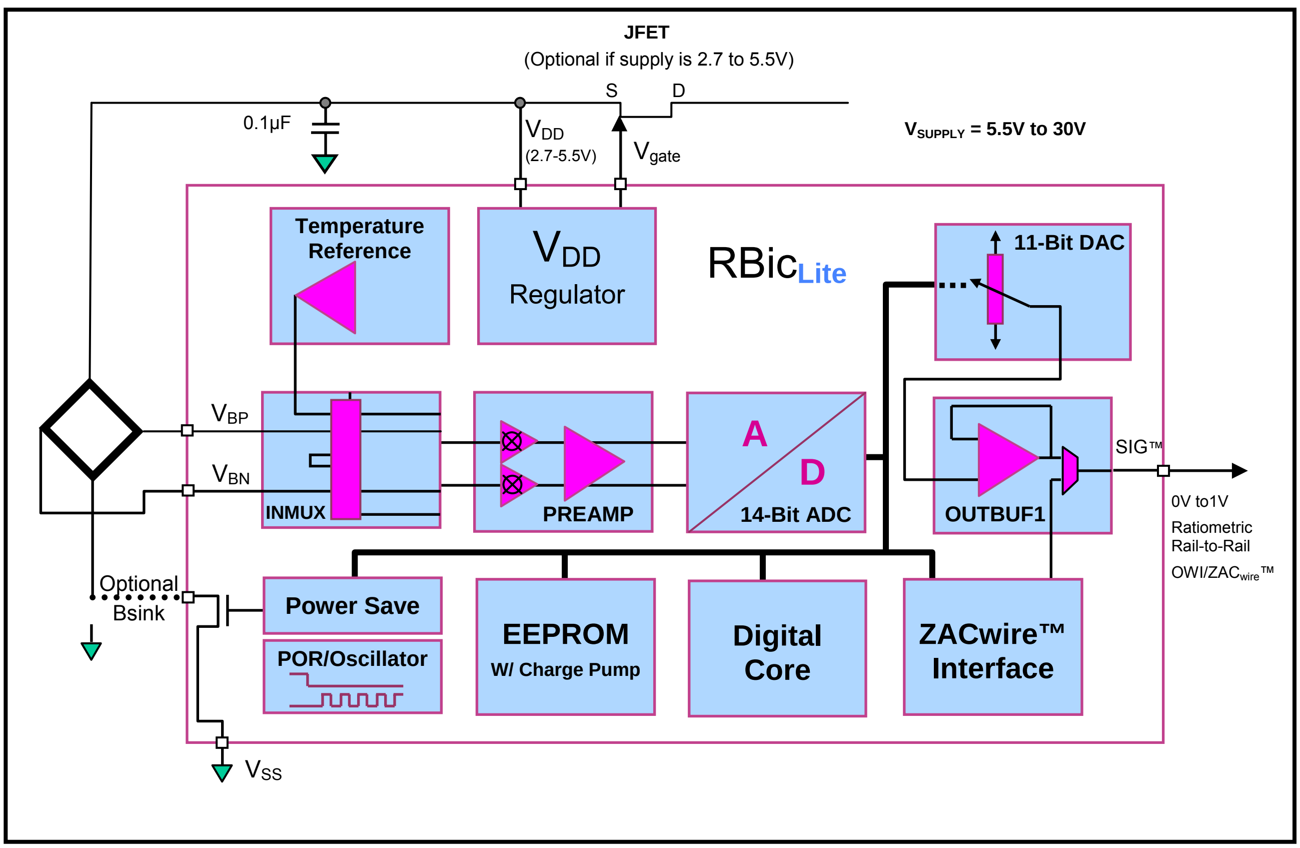


Figure 2.1 – RBic$_{Lite}$™ Block Diagram

2.2 Analog Front End

2.2.1 Bandgap/PTAT and PTAT Amplifier

The highly-linear Bandgap/PTAT provides the PTAT signal to the ADC, which allows accurate temperature conversion. In addition, the ultra-low ppm Bandgap provides a stable voltage reference over temperature for the operation of the rest of the IC.

The PTAT signal is amplified through a path in the PreAmp and fed to the ADC for conversion. The most significant 12-bits of this converted result are used for temperature measurement and temperature correction of bridge readings. When temperature is output in Digital Mode only the most significant 8-bits are given.

2.2.2 Bridge Supply

The voltage driven bridge is usually connected to V_{DD} and ground. As a power savings feature, the RBic$_{Lite}$™ also includes a switched transistor to interrupt the bridge current via pin 1 (Bsink). The transistor switching is synchronized to the A-to-D conversion and released after finishing the conversion. To utilize this feature, the low supply of the bridge should be connected to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5% or 1%.

2.2.3 PreAmp Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance designed for low noise and low drift. This PreAmp provides gain for the differential signal and re-centers its DC to $V_{DD}/2$. The output of the PreAmp block is fed into the analog-to-digital converter. The calibration sequence performed by the digital core includes an auto-zero sequence to null any drift in the PreAmp state over temperature.

The PreAmp is nominally set to a gain of 24. Other possible gain settings are 6, 12, and 48.

The inputs to the PreAmp from (VBN/VBP pins) can be reversed via an EEPROM configuration bit.

2.2.4 Analog-to-Digital Converter (ADC)

A 14-bit/1ms 2nd order charge-balancing ADC is used to convert signals coming from the PreAmp. The converter, designed in full differential switched capacitor technique, is used for converting the various signals in the digital domain. This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independent from clock frequency drift and clock jitter
- Fast conversion time owing to second order mode

Four selectable values for the zero point of the input voltage allow conversion to adapt to the sensor's offset parameter.

The conversion rate varies with the programmed update rate. The fastest conversion rate is 1k samples/s and the response time is then 1ms. Based on a best fit, the Integral Nonlinearity (INL) is less than 4 LSB$_{14Bit.}$

2.3 Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data as well as performing temperature correction and computing the temperature value for output on the digital channel.

The digital core reads correction coefficients from EEPROM and can correct for

1. Bridge Offset
2. Bridge Gain
3. Variation of Bridge Offset over Temperature (Tco)
4. Variation of Bridge Gain over Temperature (Tcg)
5. A Single Second Order Effect (SOT) (Second Order Term)

The EEPROM contains a single SOT that can be applied to correct one and only one of the following:

- 2nd Order behavior of bridge measurement
- 2nd Order behavior of Tco
- 2nd Order behavior of Tcg

(For more details, see section 3.5.1.)

If the SOT applies to correcting the bridge reading then the correction formula for the bridge reading is represented as a two step process as follows:

$$\mathbf{ZB} = \mathbf{Gain_B}[1 + \Delta\mathbf{T}*\mathbf{Tcg}]*[\mathbf{BR\_Raw} + \mathbf{Offset_B} + \Delta\mathbf{T}*\mathbf{Tco}]$$

$$\mathbf{BR} = \mathbf{ZB}*(1.25+\mathbf{SOT}*\mathbf{ZB})$$

Where:

BR	=	Corrected Bridge reading that is output as digital or analog on Sig™ pin
ZB	=	Intermediate result in the calculations
BR_Raw	=	Raw Bridge reading from ADC
T_Raw	=	Raw Temp reading converted from PTAT signal
Gain_B	=	Bridge gain term
Offset_B	=	Bridge offset term
Tcg	=	Temperature coefficient gain
Tco	=	Temperature coefficient offset
ΔT	=	(**T_Raw** - $\mathbf{T_{SETL}}$)
T_Raw	=	Raw Temp reading converted from PTAT signal
$\mathbf{T_{SETL}}$	=	T_Raw reading at which low calibration was performed (typically 25C)
SOT	=	Second Order Term

Note: See section 3.5.2.7 for limitations when SOT applies to the bridge reading.

If the **SOT** applies to correcting 2nd Order behavior of **Tco** then the formula for bridge correction is as follows:

$$\mathbf{BR} = \mathbf{Gain\_B[1 + \Delta T*Tcg]*[BR\_Raw + Offset\_B + \Delta T(SOT*\Delta T + Tco)]}$$

Note: See section 3.5.2.7 for limitations when SOT applies to Tco.

If the SOT applies to correcting 2nd Order behavior of Tcg then the formula for bridge correction is as follows:

BR = Gain_B[1 + ΔT(SOT*ΔT + Tcg)]*[BR_Raw + Offset_B_ + ΔT*Tco)]

The bandgap reference gives a very linear PTAT signal, so temperature correction can always simply be accomplished with a linear gain and offset term.

Corrected Temp Reading:

T = Gain_T*[T_Raw + Offset_T]

Where

T_Raw = Raw Temp reading converted from PTAT signal
Offset_T = TempSensor offset coefficient
Gain_T = TempSensor gain coefficient

2.3.1 EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. When programming the EEPROM, an internal charge pump voltage is used so a high voltage supply is not needed. The EEPROM is implemented as a shift register. During an EEPROM read, the contents are shifted 8 bits before each transmission of one byte occurs.

The charge pump is internally regulated to 12.5V and the programming time is typically 6ms.

Note: EEPROM writing can only be performed at temperatures lower then 85ºC.

2.3.2 One-Wire Interface - ZACwire™

The IC communicates via a one-wire serial interface. There are different commands available for the following:

- Reading the conversion result of the ADC (Get_BR_Raw, Get_T_Raw)
- Calibration commands
- Reading from the EEPROM (dump of entire contents)
- Writing to the EEPROM (trim setting, configuration, and coefficients)

2.4 Output Stage

2.4.1 Digital to Analog Converter (Output DAC)

An 11-bit DAC based on sub-ranging resistor strings is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Selection during calibration configures the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption.

Figure 2.2 shows the data timing of the DAC output with the 1kHz update rate setting.

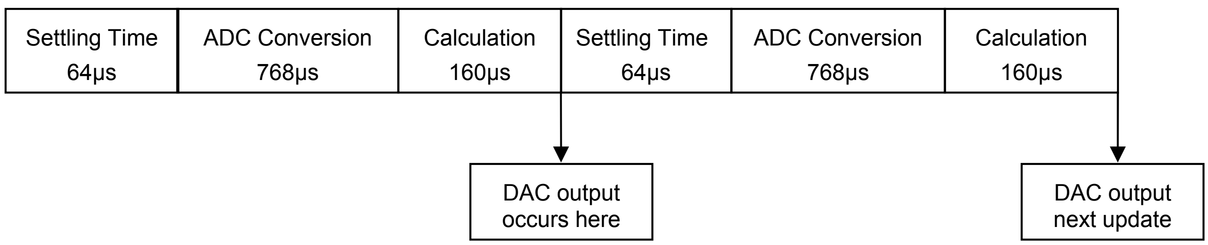


Figure 2.2 – DAC Output Timing for Highest Update Rate

2.4.2 Output Buffer

A rail-to-rail op amp configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 2.5kΩ and capacitances up to 15nF. In addition, to limit the error due to amplifier offset voltage, an error compensation circuit is included which tracks and reduces offset voltage to < 1mV.

2.4.3 Voltage Reference Block

A linear regulator control circuit is included in the Voltage Reference Block to interface with an external JFET to allow operation in systems where the supply voltage exceeds 5.5V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjustment via an EEPROM bit (see section 2.3.1) that can adjust the set point around 5.0 or 5.5V. In addition, the 1V trim setting (see below) can also act as a fine adjustment for the regulation set point.

Note: If using the external JFET for over-voltage protection purposes (i.e., 5V at JFET drain and expecting 5V at JFET source), there will be a voltage drop across the JFET; therefore ratiometricity will be compromised somewhat depending on the rds(on) of the chosen JFET. A Vishay J107 is the best choice because it has only an 8mV drop worst case. If using as regulation instead of over-voltage, a MMBF4392 also works well.

The Voltage Reference Block uses the absolute reference voltage provided by the Bandgap to produce two regulated on-chip voltage references. A 1V reference is used for the output DAC high reference when the part is configured for 0-1V analog output. For this reason, the 1V reference must be very accurate and includes trim so that its value can be trimmed within +/-3mV of 1.00V. The 1V reference is also used as the on-chip reference for the JFET regulator block so the regulation set point of the JFET regulator can be fine tuned using the 1V trim. The 5V reference can be trimmed within +/-15mV. The following table shows the order of trim codes with 0111 for the lowest reference voltage and 1000 for the highest reference voltage.

1V Reference Trim (1V vs. Trim for Nominal Process Run)

1Vref/ 5Vref__trim3	1Vref 5Vref_trim2	1Vreft 5Vref_trim1	1Vref 5Vref_trim0
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1

2.5 Clock Generator / Power On Reset (CLKPOR)

If the power supply exceeds 2.5V (maximum), the reset signal de-asserts and the clock generator starts operating at a frequency of approximately 512kHz (+17% / -22%). The exact value only influences the conversion cycle time and communication to the outside world but not the accuracy of signal processing. In addition, to minimize the oscillator error as the V_{DD} voltage changes, an on-chip regulator is used to supply the oscillator block.

2.5.1 Trimming the Oscillator

Trimming is performed at wafer level, and it is strongly recommended that this not be changed during calibration because ZACwire™ communication is no longer guaranteed at different oscillator frequencies.

Trimming Bits	Delta Frequency (KHz)
100	+385
101	+235
110	+140
111	+65
000	Nominal
001	-40
010	-76
011	-110

Example: Programming “011” → the trimmed frequency = nominal value – 110kHz

3 Functional Description

3.1 General Working Mode

The command/data transfer takes place via the one-wire Sig™ pin using the ZACwire™ serial communication protocol.

After power-on, the IC waits for 6ms (i.e., the command window) for the Start_CM command.

Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted, and the corrected values are presented on the output in analog or digital format (depending on the configuration stored in EEPROM).

Command Mode (CM) can only be entered during the 6ms command window after power-on. If the IC receives the Start_CM command during the command window, it remains in the Command Mode. The CM allows changing to one of the other modes via command. After command Start_RW, the IC is in the Raw Mode (RM). Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by power-off. Raw Mode is used by the calibration software for collection of raw bridge and temperature data so the correction coefficients can be calculated.

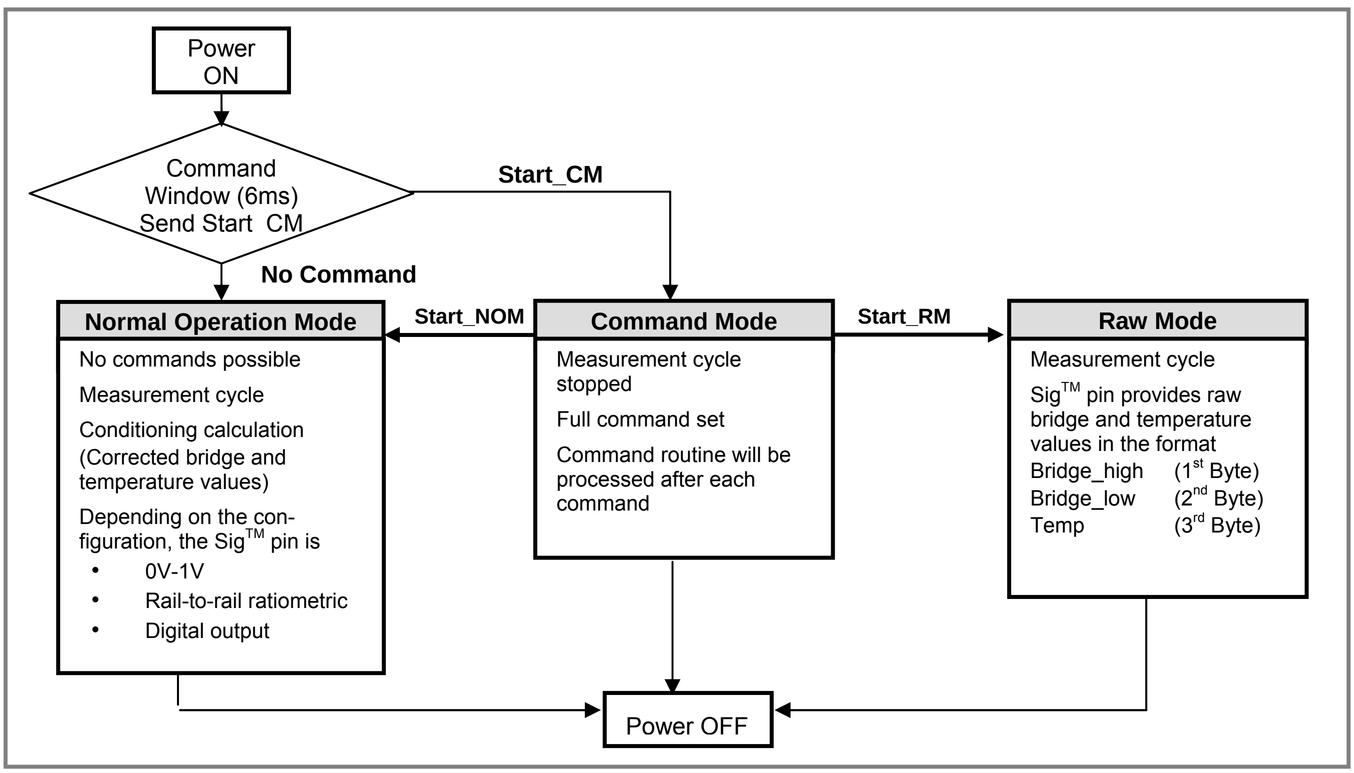


Figure 3.1 – General Working Mode

3.2 ZACwire™ Communication Interface

3.2.1 Properties and Parameters

	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	Pull-up resistor (on-chip)	$R_{ZAC,pu}$		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during CM Mode (first 6ms power up)
2	Pull-up resistor (external)	R_{ZAC,pu_ext}	150			Ω	If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150 Ω must be connected.
3	ZACwire™ rise time	$T_{ZAC,rise}$			5	µs	Any user RC network included in Sig™ path must meet this rise time
4	ZACwire™ line resistance	$R_{ZAC,line}$			3.9[1]	kΩ	Also see section 1.3
5	ZACwire™ load capacitance	$C_{ZAC,load}$	0	1	15[1]	nF	Also see section 1.3
6	Voltage level - low	$V_{ZAC,low}$		0	0.2	V_{DD}	Rail-to-rail CMOS driver
7	Voltage level - high	$V_{ZAC,high}$	0.8	1		V_{DD}	Rail-to-rail CMOS driver

[1] *The rise time must be $T_{ZAC,rise} = 2 R_{ZAC,line} * C_{ZACload} \leq 5\mu s$. If using a pull up resistor instead of a line resistor, it must meet this specification.*

3.2.2 Bit Encoding

Start bit => 50% duty cycle used to set up strobe time

Logic 1 => 75% duty cycle

Logic 0 => 25% duty cycle

Stop Bit
For the time of a half a bit width, the signal level is high. There is a half stop bit time between bytes in a packet.

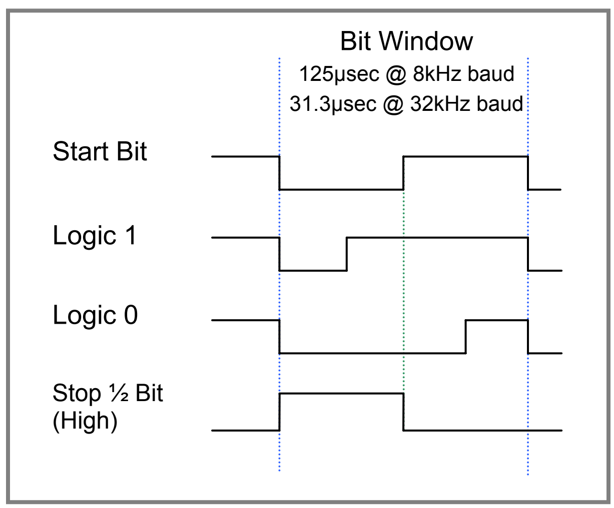


Figure 3.2 – Duty Cycle Manchester

3.2.3 Write Operation from Master to RBic$_{Lite}$™

The calibration master sends a 19-bit packet frame to the IC.

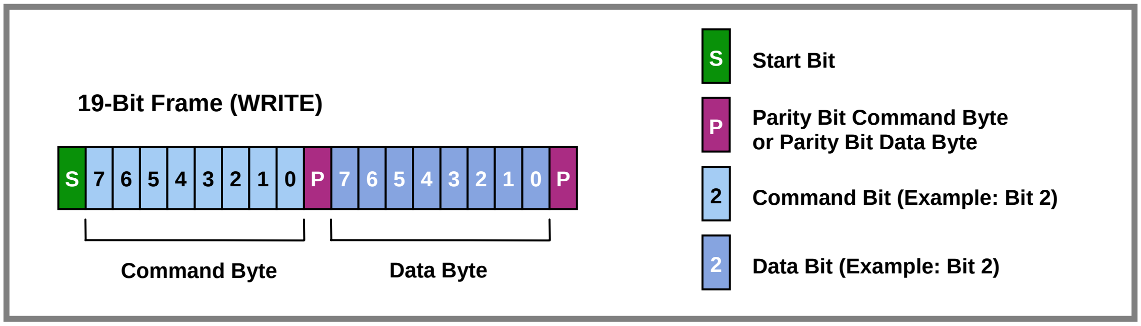


Figure 3.3 – 19-Bit Write Frame

The incoming serial signal will be sampled at a 512kHz clock rate. This protocol is very tolerant to clock skew and can easily tolerate baud rates in the 6kHz to 48kHz range.

3.2.4 RBIC$_{Lite}$™ READ Operations

The incoming frame will be checked for proper parity on both command and data bytes, as well as for any edge timeouts prior to a full frame being received.

Once a command/data pair is received, the RBic$_{Lite}$™ will perform that command. Once the command has been successfully executed by the IC, it will acknowledge success by a transmission of an A5H byte back to the master. If the master does not receive an A5H transmission within 130msec of issuing the command, it must assume the command was either improperly received or could not be executed.

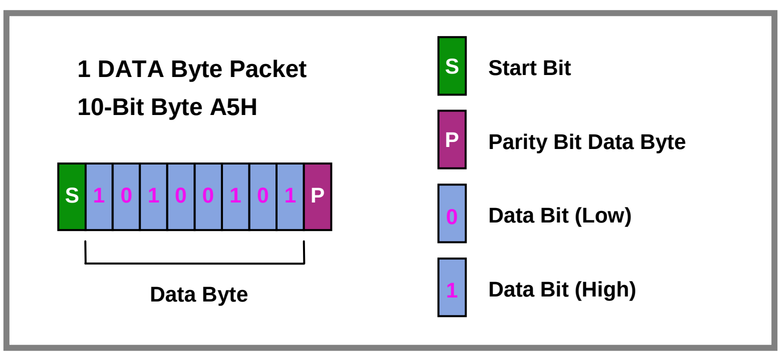


Figure 3.4 – Read Acknowledge

The RBic$_{Lite}$™ transmits 10-bit bytes (1 start bit, 8 data, 1 parity). During calibration and configuration, transmissions are normally either A5H or data. A5H indicates successful completion of a command. There are two different digital output modes configurable (digital output with temperature and digital output with only bridge data). During Normal Operation Mode, if the part is configured for digital output of the bridge reading, it first transmits the high byte of bridge data followed by the low byte. The bridge data is 14-bits in resolution, so the upper two bits of the high byte are always zero padded. There is a half stop bit time between bytes in a packet. That means for the time of a half a bit width, the signal level is high.

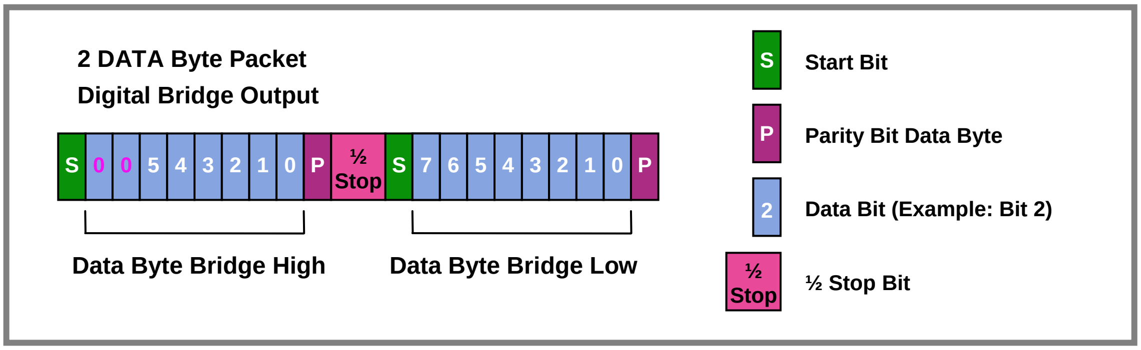


Figure 3.5 – Digital Output (NOM) Bridge Readings

The second digital output mode is digital output bridge reading with temperature. It will be transmitted as a 3-data-byte packet. The temperature byte represents an 8-bit temperature quantity spanning from –50°C to 150°C.

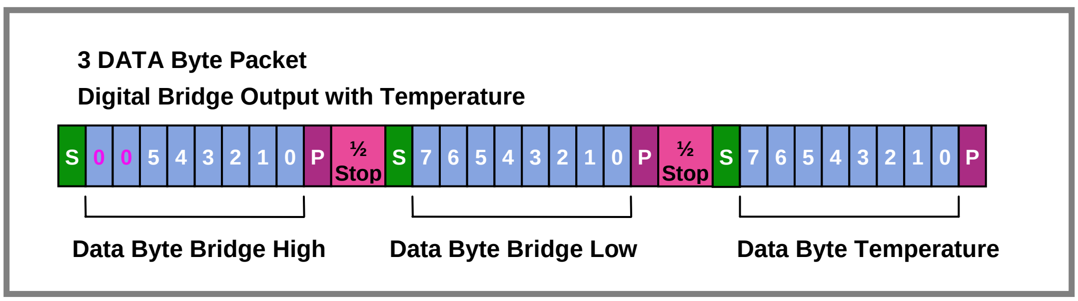


Figure 3.6 – Digital Output (NOM) Bridge Readings with Temperature

The EEPROM transmission occurs in a packet with 14 data bytes as shown in Figure 3.7.

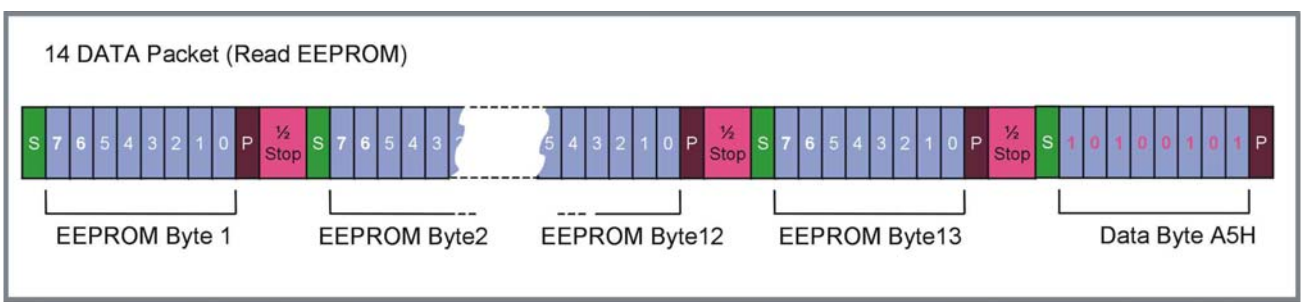


Figure 3.7 – Read EEPROM Contents

There is a variable idle time between packets. This idle time varies with the update rate setting in EEPROM.

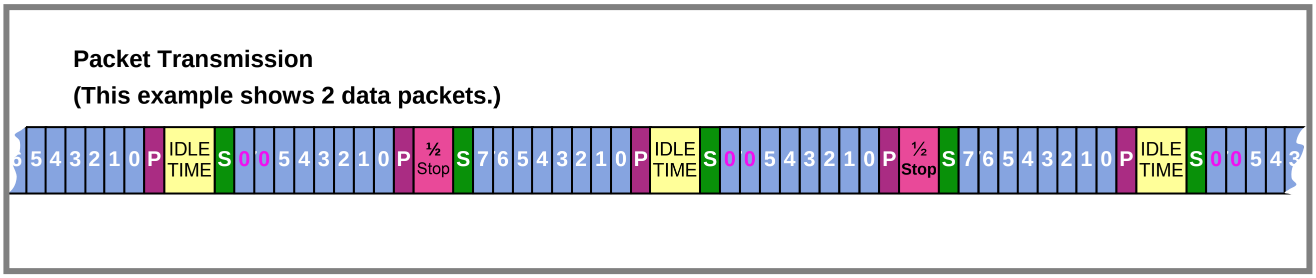


Figure 3.8 – Transmission of a Number of Data Packets

The table below shows the idle time between packets versus update rate. This idle time can vary by nominal +/-15% between parts and over a temperature range of –50°C to 150ºC.

Update Rate Setting	Idle Time between Packets
00	1ms
01	4.85ms
10	22.5ms
11	118ms

Transmissions from the IC occur at one of two speeds depending on the update rate programmed in EEPROM. If the user chooses one of the two fastest update rates (1ms or 5ms) then the baud rate of digital transmission will be 32kHz. If however, the user chooses one of the two slower update rates (25ms or 125ms), then the baud rate of digital transmission will be 8kHz.

The total transmission time for both digital output configurations is shown in Table 3.1.

Table 3.1 – Total Transmission Time for Different Update Rate Settings and Output Configuration

Update Rate	Baud Rate	Idle Time	Transmission Time – Bridge Only Readings			Transmission Time – Bridge & Temperature Readings		
1ms (1kHz)	32kHz	1.00ms	20.5 bits	31.30µs	1.64ms	31.0 bits	31.30µs	1.97ms
5ms (200Hz)	32kHz	4.85ms	20.5 bits	31.30µs	5.49ms	31.0 bits	31.30µs	5.82ms
25ms (40Hz)	8kHz	22.50ms	20.5 bits	125.00µs	25.06ms	31.0 bits	125.00µs	26.38ms
125ms (8Hz)	8kHz	118.00ms	20.5 bits	125.00µs	120.56ms	31.0 bits	125.00µs	121.88ms

It is easy to program any standard µcontroller to communicate with the RBic$_{Lite}$™. ZMDA can provide sample code for a MicroChip PIC µController.

For update rates less than 1kHz, the output is followed by a power-down as shown in Figure 3.9.

Calculation 160µs	ZACwire™ Output	Power Down Determined by Update Rate	Power-On Settling 128µs	Settling Time 64µs	ADC Conversion 768µs	Calculation 160µs	ZACwire™ Output

Figure 3.9 – ZACwire™ Output Timing for Lower Update Rates

3.2.5 High Level Protocol

The RBic$_{Lite}$™ will listen for a command/data pair to be transmitted for the 6ms after the de-assertion of its internal Power-On Reset (POR). If a transmission is not received within this time frame, then it will transition to Normal Operation Mode (NOM). In NOM, it will output bridge data in 0-1V analog, rail-to-rail ratiometric analog output, or digital depending on how the part is currently configured.

If the RBic$_{Lite}$™ receives a Start CM command within the first 6ms after the de-assertion of POR, then it will go into Command Mode (CM). In this mode, calibration/configuration commands will be executed. The RBic$_{Lite}$™ will acknowledge successful execution of commands by transmission of an A5H. The calibrating/configuring master will know a command was not successfully executed if no response is received after 130ms of issuing the command. Once in command interpreting/executing mode, the RBic$_{Lite}$™ will stay in this mode until power is removed, or a Start NOM (Start Normal Operation Mode) command is received. The START CM command is used as an interlock mechanism to prevent a spurious entry into command mode on power-up. The first command received within the 6ms window of POR must be a START CM command to enter into command interpreting mode. Any other commands will be ignored.

3.3 Command/Data Pair Encoding

The 16-bit command/data stream sent to the RBic$_{Lite}$™ can be broken into four 4-bit nibbles. The most significant two nibbles encode the command. The last two nibbles encode the data byte. (H=Hex)

Command Byte	Data	Description
00H	XXH	Read EEPROM command via Sig™ pin.[1]
20H	5XH	Enter Test Mode (Subset of Command Mode for test purposes only): Sig™ pin will assume the value of different internal test points, depending on the most significant nibble of data sent. DAC Ramp Test Mode. Gain_B[13:3] contains the starting point, and the increment is (Offset_B/8). The increment will be added every 125µsec.

[1] For more details, refer to section 3.6.

<table>
<tr><th>Command Byte</th><th>Data</th><th>Description</th></tr>
<tr><td>30H

X => Don't care

H => Hex</td><td>WDH

W => What

D => Data

H => Hex</td><td>Trim/Configure: 3rd nibble determines what is trimmed/configured.
4th nibble is data to be programmed.
<table>
<tr><th>3rd Nibble</th><th>4th Nibble Data</th><th>Description</th></tr>
<tr><td>0H</td><td>XH</td><td>Trim oscillator least significant 3 bits of data used.</td></tr>
<tr><td>1H</td><td>XH</td><td>Trim 1V reference. Least significant 4 bits of data used.</td></tr>
<tr><td>2H</td><td>XH</td><td>Offset Mode. Least significant 2 bits of data used.</td></tr>
<tr><td>3H</td><td>XH</td><td>Set output mode. Least significant 2 bits used.</td></tr>
<tr><td>4H</td><td>XH</td><td>Set update rate. Least significant 2 bits used.</td></tr>
<tr><td>5H</td><td>XH</td><td>Configure JFET regulation.</td></tr>
<tr><td>6H</td><td>XH</td><td>Program the Tc_cfg register. Least significant 3-bits used. Most significant bit of data nibble should be 0.</td></tr>
<tr><td>7H</td><td>XH</td><td>Program bits [99:96] of EEPROM. {SOT_cfg,Pamp_Gain}</td></tr>
</table></td></tr>
<tr><td>40H</td><td>00H</td><td>Start NOM => Ends Command Mode, transition to Normal Operation Mode</td></tr>
<tr><td>40H</td><td>10H</td><td>Start Raw Mode (RM)
In this mode if Gain_B = 800H and Gain_T = 80H, then the digital output will simply be the raw values of the ADC for the Bridge reading, and the PTAT conversion.</td></tr>
<tr><td>50H</td><td>00H</td><td>START CM => Start the Command Mode; used to enter command interpret mode.</td></tr>
<tr><td>60H</td><td>YYH</td><td>Program SOT (2nd Order Term)</td></tr>
<tr><td>70H</td><td>YYH</td><td>Program T_{SETL}</td></tr>
<tr><td>80H</td><td>YYH</td><td>Program Gain_B upper 7 bits (Set MSB of YY to 0.)</td></tr>
<tr><td>90H</td><td>YYH</td><td>Program Gain_B lower 8 bits</td></tr>
<tr><td>A0H</td><td>YYH</td><td>Program Offset_B upper 6 bits (Set two MSBs of YY to 0.)</td></tr>
<tr><td>B0H</td><td>YYH</td><td>Program Offset_B lower 8 bits</td></tr>
<tr><td>C0H</td><td>YYH</td><td>Program Gain_T</td></tr>
<tr><td>D0H</td><td>YYH</td><td>Program Offset_T</td></tr>
<tr><td>E0H</td><td>YYH</td><td>Program Tco</td></tr>
<tr><td>F0H</td><td>YYH</td><td>Program Tcg</td></tr>
</table>

*SDO: Scan Data Out

Calibration Sequence

Although the RBic$_{Lite}$™ can function with many different types of resistive bridges, assume it is connected to a pressure bridge for the following calibration example.

In this case, calibration essentially involves collecting raw bridge and temperature data from the RBic$_{Lite}$™ for different known pressures and temperatures. This raw data can then be processed by the calibration master (the PC), and the calculated coefficients can then be written to the EEPROM of the RBic$_{Lite}$™.

ZMDA can provide software and hardware with samples to perform the calibration.

There are three main steps to calibration:

1. Assigning a unique identification to the IC. This identification is programmed in EEPROM and can be used as an index into the database stored on the calibration PC. This database will contain all the raw values of bridge readings and temp reading for that part, as well as the known pressure and temperature the bridge was exposed to. This unique identification can be stored in a combination of the following EEPROM registers T_{SETL}, Tcg, Tco. These registers will be overwritten at the end of the calibration process, so this unique identification is not a permanent serial number.
2. Data collection. Data collection involves getting raw data from the bridge at different known pressures and temperatures. This data is then stored on the calibration PC using the unique identification of the IC as the index to the database.
3. Coefficient calculation and write. Once enough data points have been collected to calculate all the desired coefficients then the coefficients can be calculated by the calibrating PC and written to the IC.

Step 1 Assigning Unique Identification

Assigning a unique identification number is as simple as using the commands Program TSETL, Program Tcg, and Program Tco. These 3 8-bit registers will allow for 16M unique devices. In addition Gain_B must be programmed to 800H (unity) and Gain_T must be programmed to 80H (unity).

Step 2 Data Collection

The number of different unique (pressure, temperature) points that calibration needs to be performed at depends on the customer's needs. The minimum is a 2-point calibration, and the maximum is a 5-point calibration. To acquire raw data from the part, instruct the RBic$_{Lite}$™ to enter Raw Mode. This is done by issuing a Start CM (Start Command Mode 5000H) command to the IC followed by a Start RM (Start Raw Mode 4010H) command with the LSB of the upper data nibble set. Now if the Gain_B term was set to unity (800H) and the Gain_T term was also set to unity (80H) then the part will be in the Raw Mode and will be outputting raw data on its Sig™ pin instead of corrected bridge and temperature. The calibration system should now collect several of these data points (16 each of bridge and temperature is recommended) and average them. These raw bridge and temperature measurements should be stored in the database along with the known pressure and temperature. The output format during Raw Mode is Bridge_High, Bridge_Low, Temp, each of these being 8-bit quantities. The upper 2-bits of Bridge_High are zero-filled. The Temp data (8-bits only) would not really be enough data for accurate temperature calibration. Therefore the upper 3 bits of temperature information are not given, but rather assumed known. Therefore effectively 11 bits of temperature information are provided in this mode.

Step 3 Coefficient Calculations

The math to perform the coefficient calculation is very complicated and will not be discussed in detail. There is a rough overview in the "Calibration Math" section. Rather ZMD will provide software to perform the coefficient calculation. ZMD can also provide source code of the algorithms in a C code format. Once the coefficients are calculated the final step is to write them to the EEPROM of the RBic$_{Lite}$™.

The number of calibration points required can be as few as two or as many as five. This depends on the precision desired, and the behavior of the resistive bridge in use.

1. 2-point calibration would be used to obtain only a gain and offset term for bridge compensation with no temperature compensation for either term.
2. 3-point calibration would be used to also obtain the Tco term for 1st order temperature compensation of the bridge offset term.
3. 3-point calibration could also be used to obtain the additional term SOT for 2nd order correction for the bridge (SOT_BR), but no temperature compensation of the bridge output.[1]
4. 4-point calibration would be used to also obtain both the Tco term and the Tcg term, which provides 1st order temperature compensation of the bridge offset gain term.
5. 4-point calibration could also be used to obtain the Tco term and the SOT_BR term.[1]
6. 5-point calibration would be used to obtain Tco, Tcg and an SOT term that provides 2nd order correction applied to one and only one of the following: 2nd order Tco (SOT_Tco), 2nd order Tcg (SOT_Tcg), or 2nd order bridge (SOT_BR). [1]

[1] See section 3.5.2.7 for limitations.

3.4 EEPROM Bits

Programmed through the serial interface:

EEPROM Range	Description	Note
2:0	Osc_Trim	See the table in section 2.5.1 for complete data. 100 => Fastest 101 => 3 clicks faster than nominal 110 => 2 clicks faster than nominal 111 => 1 click faster than nominal 000 => Nominal 001 => 1 click slower than nominal 010 => 2 clicks slower than nominal 011 => Slowest
6:3	1V_Trim/JFET_Trim	See the table in section 2.4.3.
8:7	A2D_Offset	Offset selection: 11 => [-1/2,1/2] mode bridge inputs 10 => [-1/4,3/4] mode bridge inputs 01 => [-1/8,7/8] mode bridge inputs 00 => [-1/16,15/16] mode bridge inputs To change the bridge signal polarity, set Tc_cfg[3](=Bit 87).
10:9	Output_Select	00 => Digital (3-bytes with parity) Bridge High {00,[5:0]} Bridge Low [7:0] Temp [7:0] 01 => 0-1V Analog 10 => Rail-to-rail ratiometric analog output 11 => Digital (2-bytes with parity) (No Temp) Bridge High {00,[5:0]} Bridge Low [7:0]
12:11	Update_Rate	00 => 1 msec (1kHz) 01 => 5 msec (200Hz) 10 => 25 msec (40Hz) 11 => 125 msec (8 Hz)

EEPROM Range	Description	Note
14:13	JFET_Cfg	00 => No JFET regulation (lower power) 01 => No JFET regulation (lower power) 10 => JFET regulation centered around 5.0V 11 => JFET regulation centered around 5.5V (i.e. over-voltage protection).
29:15	Gain_B	Bridge Gain: Gain_B[14] => mult x 8 Gain_B[13:0] => 14-bit unsigned number representing a number in the range [0,8).
43:30	Offset_B	Signed 14-bit offset for bridge correction
51:44	Gain_T	Temperature gain coefficient used to correct PTAT reading.
59:52	Offset_T	Temperature offset coefficient used to correct PTAT reading.
67:60	T_{SETL}	Stores Raw PTAT reading at temperature in which low calibration points were taken.
75:68	Tcg	Coefficient for temperature correction of bridge gain term. Tcg = 8-bit magnitude of Tcg term. Sign is determined by Tc_cfg (bits 87:84).
83:76	Tco	Coefficient for temperature correction of bridge offset term. Tco = 8-bit magnitude of Tco term. Sign and scaling are determined by Tc_cfg (bits 87:84).
87:84	Tc_cfg	This 4-bit term determines options for Temperature compensation of the bridge. Tc_cfg[3] => If set, Bridge Signal Polarity flips. Tc_cfg[2] => If set, Tcg is negative. Tc_cfg[1] => Scale magnitude of Tco term by 8, and if SOT applies to Tco, scale SOT by 8. Tc_cfg[0] => If set, Tco is negative.
95:88	SOT	2nd Order Term. This term is a 7-bit magnitude with sign. SOT[7] = 1 ➔ negative SOT[7] = 0 ➔ positive SOT[6:0] = magnitude [0-127] This term can apply to a 2nd order Tcg, Tco or bridge correction[1]. (See Tc_cfg above.)

[1] The SOT range for the bridge correction is limited for the negative value to 0xC0 by the MathLib.DLL.

EEPROM Range	Description	Note
99:96	{SOT_cfg, Pamp_Gain}	Bits [99:98] = SOT_cfg (For more details, see section 3.5.1.) 00 = SOT applies to Bridge 01 = SOT applies to Tcg 10 = SOT applies to Tco 11 = Prohibited Bits [97:96] = PreAmp Gain 00 => 6 01 => 24 (default setting) 10 => 12 11 => 48 (Only the default gain setting (24) is tested at the factory; all other gain settings are not guaranteed.)

3.5 Calibration Math

3.5.1 Correction Coefficients

(All terms are calculated external to the DUT and then programmed to EEPROM through serial interface.)

Gain_B = Gain term used to compensate span of Bridge reading.

Offset_B= Offset term used to compensate offset of Bridge reading.

Gain_T = Gain term used to compensate span of Temp reading.

Offset_T = Offset term used to compensate offset of Temp reading.

SOT = Second Order Term. This term can be used applied as a second order correction term for

1. The bridge measurement
2. Temperature coefficient of offset (Tco)
3. Temperature coefficient of gain (Tcg)

EEPROM bits 99:98 determine what SOT applies to.

Note: There are limitations for the SOT for the bridge measurement and for the SOT for the Tco which are explained in section 3.5.2.7.

T_{SETL} = RAW PTAT reading at low temperature at which calibration was performed (typically room temp)

Tcg = Temperature correction coefficient of bridge gain term
This term has an 8-bit magnitude and a sign bit (Tc_cfg[2]).

Tco = Temperature correction coefficient of bridge offset term
This term has an 8-bit magnitude, a sign bit (Tc_cfg[0]) and a scaling bit (Tc_cfg[1])which can multiply its magnitude by 8.

3.5.2 Interpretation of Binary Numbers for Correction Coefficients

BR_Raw should be interpreted as an unsigned number in the set [0,16383] with resolution of 1.

T_Raw should be interpreted as an unsigned number in the set [0,16383] with resolution of 4.

3.5.2.1 Gain_B Interpretation

Gain_B should be interpreted as a number in the set [0,64). The MSB (bit 14) is a scaling bit that will multiply the effect of the remaining bits Gain_B[13:0] by 8. Bits Gain_B[13:0] represent a number in the range of [0,8) with Gain_B[13] having a weighting of 4 and each subsequent bit has a weighting of ½ the previous bit.

Table 3.2 – Gain_B Weightings

Bit Position	Weighting
13	4
12	2
11	1
...	...
1	2^{-10}
0	2^{-11}

Examples:

The binary number: 010010100110001 = 4.6489; the scaling number is 0 so there is no multiply by 8 of the number represented by Gain_B[13:0].

The binary number: 101100010010110 = 24.586; the scaling number is 1 so there is a multiply by 8 of the number represented by Gain_B[13:0].

Limitation: Using the 5-point calibration 5pt-Tcg&Tco&SOT_Tco (including the second order SOT_Tco), the Gain_B is limited to a value equal or less than 8 (instead of 64).

3.5.2.2 Offset_B Interpretation

Offset_B is a 14-bit signed binary number in two's complement form. The MSB has a weighting of –8192. The following bits then have a weighting of: 4096, 2048, 1024, …

Table 3.3 – Offset_B Weightings

Bit Position	Weighting
13	-8192
12	4096
11	2048
...	...
1	$2^1 = 2$
0	$2^0 = 1$

Thus the binary number: 11111111111100 = -4

3.5.2.3 Gain_T Interpretation

Gain_T should be interpreted as a number in the set [0,2). Gain_T[7] has a weighting of 1, and each subsequent bit has a weighting of ½ the previous bit.

Table 3.4 – Gain_T Weightings

Bit Position	Weighting
7	1
6	0.5
5	0.25
...	...
1	2^{-6}
0	2^{-7}

3.5.2.4 Offset_T Interpretation

Offset_T is an 8-bit signed binary number in two's complement form. The MSB has a weighting of –128. The following bits then have a weighting of: 64, 32, 16 …

Table 3.5 – Offset_T Weightings

Bit Position	Weighting
7	-128
6	64
...	...
1	$2^1 = 2$
0	$2^0 = 1$

For example, the binary number 00101001 = 41

3.5.2.5 Tco Interpretation

Tco is specified as an 8-bit magnitude with an additional sign bit (Tc_cfg[0]) and a scalar bit (Tc_cfg[1]). When the scalar bit is set, the signed Tco is multiplied by 8.

Tco Resolution: 0.175µV/V/°C (input referred)
Tco Range: +/- 44.6µV/V/°C (input referred)

If the scaling bit is used then the above resolution and range are scaled by 8 to give

Tco Scaled Resolution: 1.40µV/V/°C (input referred)
Tco Scaled Range: +/- 357µV/V/°C (input referred)

3.5.2.6 Tcg Interpretation

Tcg is specified as an 8-bit magnitude with an additional sign bit (Tc_cfg[2]).

Tcg Resolution: 17.0ppm/^{o}C

Tcg Range: +/- 4335ppm/^{o}C

3.5.2.7 SOT Interpretation

SOT is a second order term that can apply to one and only one of the following: bridge non-linearity correction, Tco non-linearity correction, or Tcg non-linearity correction.

As it applies to bridge non-linearity correction:

Resolution: 0.25% @ Full Scale

Second order correction SOT_BR is possible up to +5%/-6.2% full scale difference from the ideal fit (straight line) because the SOT coefficient values are limited to the range of (0xC0 = -0.25_{dec}) to (0x7F = 0.4960938_{dec}). (Saturation in internal arithmetic will occur at greater negative non-linearities.)

Limitation: Using any calibration method for which SOT is applied to the bridge measurement (SOT_BR), there is a possibility of calibration math overflow. This only occurs if the sensor input exceeds 200% of the calibrated full span, which means the highest applied pressure should never go higher than this value.[1]

As it applies to Tcg:

Resolution: 0.3 ppm/(^{o}C)^2

Range: +/- 38ppm/(^{o}C)^2

As it applies to Tco:

Two settings are possible. It is possible to scale the effect of SOT by 8. If Tc_cfg[1] is set, then both Tco and SOT's contribution to Tco are multiplied by 8.

Resolution at unity scaling:	1.51nV/V/(^{o}C)^2	(input referred)
Range:	+/- 0.192µV/V/(^{o}C)^2	(input referred)
Resolution at 8x scaling:	12.1nV/V/(^{o}C)^2	(input referred)
Range:	+/- 1.54µV/V/(^{o}C)^2	input referred)

Limitation: If the second order term SOT applies to Tco, the bridge gain Gain_B is limited to values equal or less than 8 (instead of 64).

[1] **Example of the Limitation When SOT is Applied to the Bridge Reading**

This example of the limitation when SOT is applied to the bridge reading uses a pressure sensor bridge that outputs -10mv at the lowest pressure of interest. That point is calibrated to read 0%. The same sensor outputs +40mV at the highest pressure of interest. That point is calibrated to read 100%.

This sensor has a 50mV span over the pressure range of interest. If the sensor were to experience an over-pressure event that took the sensor output up to 90mV (200% of span), the internal calculations could overflow. The result would be a corrected bridge reading that would not be saturated at 100% as expected but instead read a value lower than 100%. This problem only occurs when SOT is applied to correct the bridge reading.

3.6 Reading EEPROM Contents

The contents of the entire EEPROM memory can be read out using the Read EEPROM command (00H). This command will cause the IC to output consecutive bytes on the ZACwire™. After each transmission, the EEPROM contents are shifted 8 bits. The bit order of these bytes is given in Table 3.6.

Table 3.6– Read EEPROM Command Bit Order

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1:	Offset_B[7:0]							
Byte 2:	Gain_T[1:0]		Offset_B[13:8]					
Byte 3:	Offset_T[1:0]		Gain_T[7:2]					
Byte 4:	T_{SETL}[1:0]		Offset_T[7:2]					
Byte 5:	Tcg[1:0]		T_{SETL}[7:2]					
Byte 6:	Tco[1:0]		Tcg[7:2]					
Byte 7:	Tc_cfg[1:0]		Tco[7:2]					
Byte 8:	SOT[5:0]						Tc_cfg[3:2]	
Byte 9:	Osc_Trim[1:0]		SOT_cfg[3:0]*				SOT[7:6]	
Byte 10:	Output_Select[0]	A2D_offset[1:0]		1V_Trim[3:0]**				Osc_Trim[2]
Byte 11:	Gain_B[2:0]			JFET_Cfg[1:0]		Update_Rate[1:0]		Output_Select[1]
Byte 12:	Gain_B[10:3]							
Byte 13:	Offset_B[3:0]***				Gain_B[14:11]			
Byte 14:	A5H							

* SOT_cfg/Pamp_Gain
** 1V_Trim/JFET_Trim
*** Duplicates first 4 bits of Byte 1

4 Application Circuit Examples

Typical output analog load resistor R_L= 10kΩ (minimum 2.5kΩ). This optional load resistor can be configured as a pull-up or pull-down. If it is configured as a pull-down, it cannot be part of the module to be calibrated because this would prevent proper operation of the ZACwire™. If a pull-down load is desired, it must be added to system after module calibration.

There is no output load capacitance needed.

EEPROM contents: OUTPUT_select, JFET_Cfg, 1V_Trim/JFET-Trim

4.1 Three-Wire Rail-to-Rail Ratiometric Output

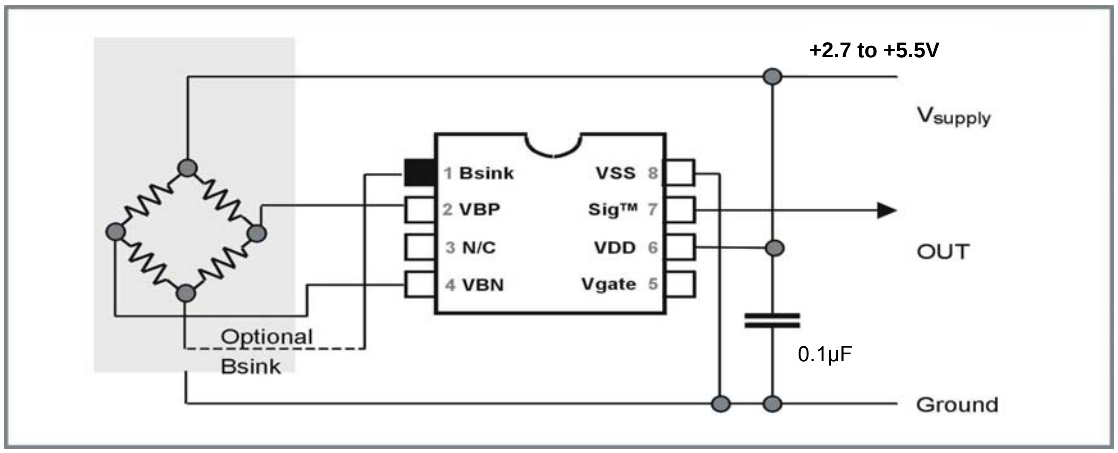


Figure 4.1 – Rail-to-Rail Ratiometric Voltage Output, Temperature Compensation via Internal PTAT

The optional bridge sink allows a power savings of bridge current. The output voltage can be either

a) Rail-to-rail ratiometric analog output V_{DD}(=Vsupply).

b) 0 to 1V analog output is also possible. The absolute voltage output reference is trimmable 1V (+/-2mV) in the 1V output mode via a 4-bit EEPROM field. (See section 2.4.3.)

4.2 Absolute Analog Voltage Output

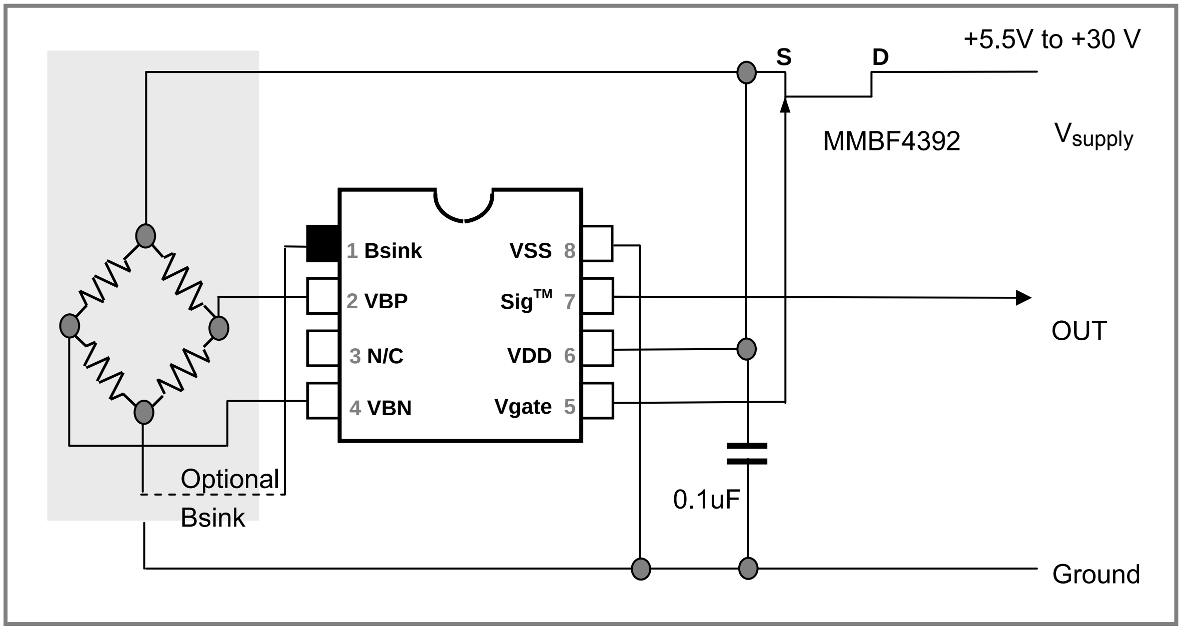


Figure 4.2 – Absolute Voltage Output with Temperature Compensation via Internal Temperature PTAT External JFET Regulation[1] for all Industry Standard Applications

The output signal range is either

a) 0 to 1V analog output. The absolute voltage output reference is trimmable 1V (+/-2mV) in the 1V output mode via a 4-bit EEPROM field. (See section 2.4.3.)

b) Rail-to-rail analog output. The on-chip reference for the JFET regulator block is trimmable 5V (+/-~10mV) in the ratiometric output mode via a 4-bit EEPROM field. (See section 2.4.3.)

[1] The gate-source cutoff voltage (V_{GS}) of the selected JFET must be ≤ -2V.

4.3 Three-Wire Ratiometric Output with Over-Voltage Protection

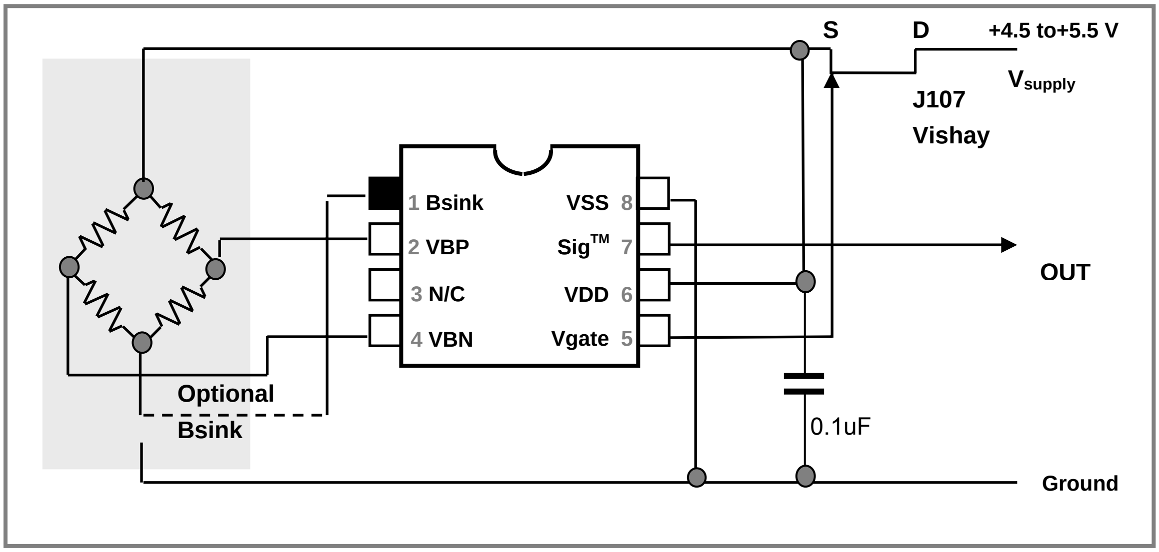


Figure 4.3 – Ratiometric Output, Temperature Compensation via Internal Diode

In this application, the JFET is used for over-voltage protection. The JFET_Cfg bits (14:13) in EEPROM are configured to 5.5V. There is an additional maximum error of 8mV caused by non-zero r_{ON} of the limiter JFET.

4.4 Digital Output

For all three circuits the output signal can also be digital. Depending from the output select bits bridge signal or the bridge signal and temperature signal are sent.

For the digital output no load resistor or load capacity are necessary. No pull down resistor is allowed. If a line resistor or pull-up resistor is used, the requirement for the rise time must be met ($\leq 5\ \mu s$). The IC output includes a pull-up resistor of about 30kΩ. The digital output can easily be read by firmware from a micro-controller and ZMD can provide the customer with software in developing the interface.

4.5 Output Short Protection

The output of the $RBic_{Lite}$™ has no short protection. Therefore, a resistor R_{SP} in series with the output must be added in the application module. Refer to Table 4.1 to determine the value of R_{SP}. To minimize additional error caused by this resistor for the analog output voltage, the load impedance must meet the following requirement:

$$R_L >> R_{SP}$$

Table 4.1 – Resistor for Short Protection

Temperature Range (T_{AMBMAX})	Resistor R_{SP}[1]
Up to 85ºC	51 Ω
Up to 125ºC	100 Ω
Up to 150 ºC	240 Ω

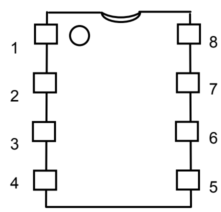
5 ESD/Latch-Up-Protection

All pins have an ESD protection of >4000V and a latch-up protection of ±100mA or of +8V/ –4V (to VSS/VSSA). ESD protection referred to the Human Body Model is tested with devices in SOP-8 packages during product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

[1] $R_{SP} = V_{DD}/I_{max}$ with $I_{max} = [(170ºC - T_{AMBMAX})/(163\ ºC/mW)] - V_{DD} * I_{DD}$

6 Pin Configuration and Package

Figure 6.1 – $RBic_{Lite}$™ Pin-Out Diagram



The standard package of the $RBic_{Lite}$™ is SOP-8 (3.81mm body (150mil) wide) with lead-pitch. 1.27mm (50mil).

Pin-No.	Name	Description
1	Bsink	Optional ground connection for bridge ground. Used for power savings
2	VBP	Positive bridge connection
3	N/C	No connection
4	VBN	Negative bridge connection
5	Vgate	Gate control for external JFET regulation/over-voltage protection
6	VDD	Supply voltage (2.7-5.5V)
7	Sig™	ZACwire™ interface (analog out, digital out, calibration interface)
8	VSS	Ground supply

7 Test

The test program is based on this datasheet. The final parameters that will be tested during series production are listed in the tables of section 1.

The digital part of the IC includes a scan path, which can be activated and controlled during wafer test. It guarantees failure coverage more than 98%. Further test support for testing of the analog parts on wafer level is included in the DSP.

8 Reliability

The $RBic_{Lite}$™ has successfully passed AEC Q100 automotive qualification testing, which includes reliability testing for the temperature range from -50 to 150ºC.

9 Customization

For high-volume applications, which require an upgraded or downgraded functionality compared to the ZM31010, ZMD can customize the circuit design by adding or removing certain functional blocks. ZMD can provide a custom solution quickly because it has a considerable library of sensor-dedicated circuitry blocks. Please contact ZMD for further information.

10 Related Documents

- ZMD31010 $RBic_{Lite}$™ *Development Kit Documentation*
- ZMD31010 $RBic_{Lite}$™ *SSC Kits Feature Sheet* (includes ordering codes and price information)
- ZMD31010 $RBic_{Lite}$™ *Errata Sheet – Rev B Production*
- ZMD31010 $RBic_{Lite}$™ *Errata Sheet – Rev A Production*
- ZMD31010 $RBic_{Lite}$™ *Application Notes – In-Circuit Programming Boards*
- ZMD31010 $RBic_{Lite}$™ *Die Dimensions and Pad Coordinates*
- ZMD31010 $RBic_{Lite}$™ *Mass Calibrator Kit Documentation*

For the most recent revisions of this document and of the related documents, please go to www.zmd.biz.

For further information:

ZMD AG
Grenzstrasse 28
01109 Dresden, Germany
Phone +49 (0)351.8822.7.772
Fax +49 (0)351.8822.87.772
sales@zmd.de
www.zmd.biz

ZMD America, Inc.
201 Old Country Road, Suite 204
Melville, NY 11747, USA
Phone +01 (631) 549-2666
Fax +01 (631) 549-2882
sales@zmda.com
www.zmd.biz

ZMD Far East
1F, No.14, Lane 268
Sec. 1 Guangfu Road
HsinChu City 300
Taiwan
Phone +886.3.563.1388
Fax +886.3.563.6385
sales@zmd.de
www.zmd.biz