ASSP
LED driver IC for lighting

MB39C601

■ DESCRIPTION

MB39C601 is a flyback type switching regulator contorller IC. The LED current is regulated by controlling the switching on-time or controlling the switching frequency, depending on the LED load. It is most suitable for the general lighting applications, for example stocks of commercial and residential light bulbs and so on.

■ FEATURES

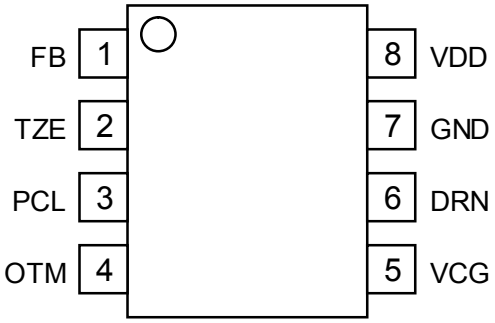
- High power factor in Single Conversion
- High efficiency and low EMI by detecting transformer zero energy
- TRIAC Dimmable LED lighting
- Control of the current of Primary Winding without the external sense resistor
- Highly efficient protective function
  - Under voltage lock out (UVLO)
  - Over load protection
  - Output over voltage protection
  - Over temperature protection
- High efficiency at the light load, at Low Power Mode (LPM) Burst Operation in switching frequency control
- Frequency setting depend on the FB pin current : 30 kHz to 130 kHz
- Input voltage range VDD : 9V to 20V
- Input voltage range for LED lighting applications : $AC110V_{RMS}$, $AC230V_{RMS}$
- Package : SOP-8 (3.9mm × 5.05mm × 1.75mm [Max])

■ APPLICATIONS

- LED lighting
- TRIAC dimmable LED lighting etc

■ PIN ASSIGNMENT

(TOP VIEW)

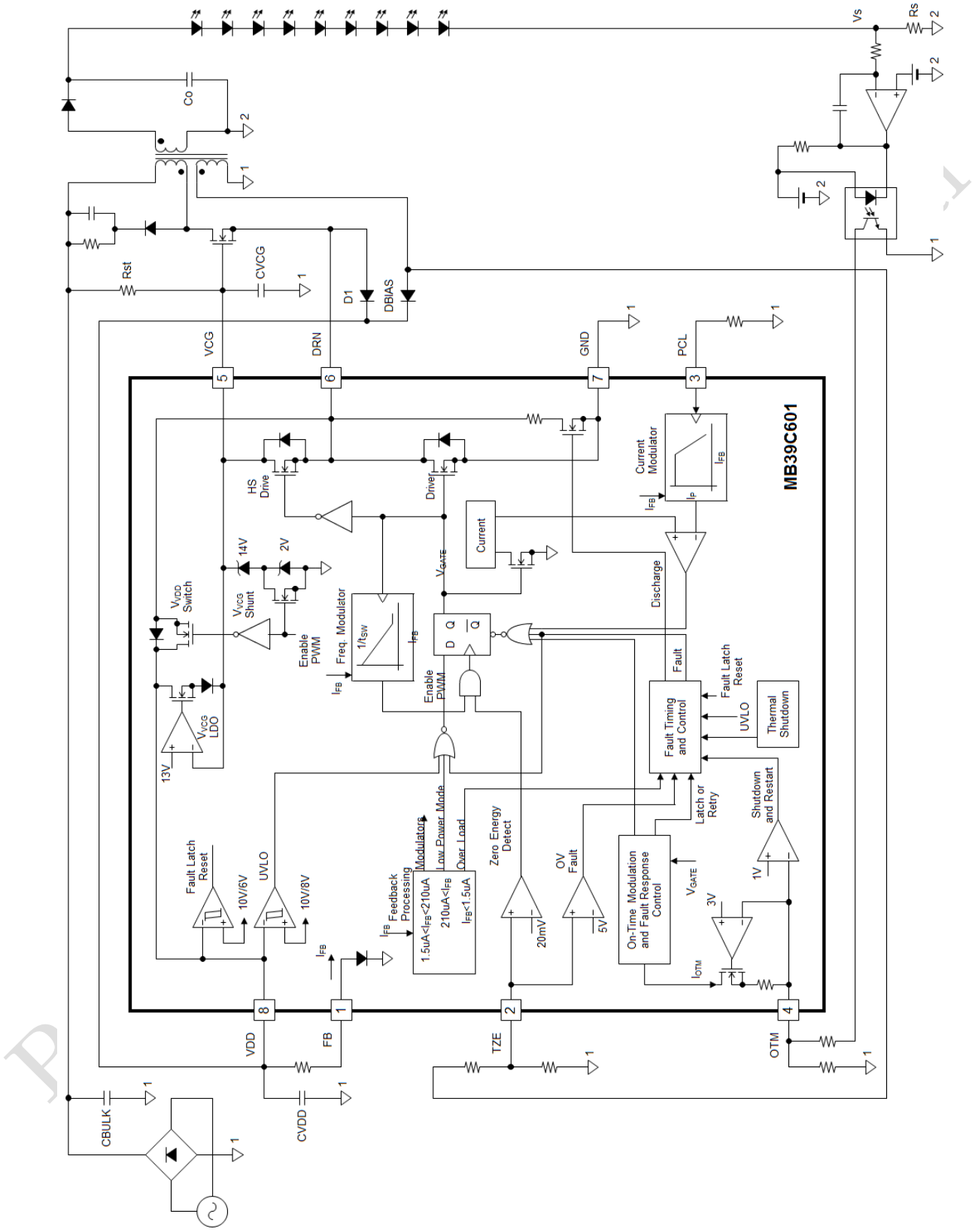


(FPT-8P-M02)

■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	FB	I	Switching frequency setting pin.
2	TZE	I	Transformer zero energy detecting pin.
3	PCL	I	Pin for controlling peak current of transformer primary winding.
4	OTM	I	On-time setting pin.
5	VCG	-	External MOSFET gate bias pin.
6	DRN	O	External MOSFET source connection pin.
7	GND	-	Ground pin.
8	VDD	-	Power supply pin.

■ BLOCK DIAGRAM (On-time control application)



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	MIN	MAX	Unit
VDD pin input voltage	V_{VDD}	VDD pin	-0.3	25	V
Input voltage	V_{DRN}	DRN pin	-	20	V
	V_{VCG}	VCG pin	-0.3	16	V
	V_{TZE}	TZE pin	-0.3	6.0	V
	V_{OTM}	OTM pin	-0.3	6.0	V
	V_{PCL}	PCL pin	-0.3	6.0	V
	V_{FB}	FB pin	-0.3	2.0	V
Input current	I_{VCG}	VCG pin	-	10	mA
	I_{OTM}	OTM pin	-1	0	mA
	I_{PCL}	PCL pin	-1	0	mA
	I_{FB}	FB pin	0	1	mA
Output current	I_{DRN}	DRN pin	-	4	A
	I_{DRN}	DRN pin Pulsed 200ns, 2% duty cycle	-0.01	4.5	A
Power dissipation	P_D	Ta≤ 25°C	-	800 *1	mW
Storage temperature	T_{STG}		-55	+125	°C

*1: The value when using two layers PCB.
Referrence : θja(wind speed 0m/s) : 125°C/W

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
VDD pin input voltage	VDD	VDD pin	9	-	20	V
VCG pin input voltage	VCG	VCG pin	9	-	13	V
VCG pin input current	I_{VCG}	VCG pin	10	-	2000	uA
OTM pin resistance	R_{OTM}	OTM pin Shutdown / retry mode	25	-	100	kΩ
		OTM pin Latch - off mode	150	-	750	kΩ
PCL pin resistance	R_{PCL}	PCL pin	24.3	-	100	kΩ
TZE pin resistance	R_{TZE}	TZE pin	50	-	200	kΩ
VCG pin capacitance	C_{VCG}	VCG pin	33	-	200	nF
VDD pin capacitance	C_{BP}	Ceramic capacitance to set between VDD and GND pin	0.1	-	1	uF
Operating ambient temperature	Ta	-	-40	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{VDD} = 12V)

Parameter	Symbol	Pin No.	Condition	MIN	TYP	MAX	Unit
1. VDD and VCG SUPPLY							
VCG output voltage (Operating)	$VCG_{(OPER-ATING)}$	5	V_{VDD}=14V, I_{VCG}=2.0mA	13	14	15	V
VCG output voltage (Disable)	$VCG_{(DISA-BLED)}$	5	V_{VDD}=12V, I_{VCG}=26uA, I_{FB}=350uA	15	16	17	V
VCG output voltage difference	ΔVCG	5	$VCG_{(DISABLED)}$ – $VCG_{(OPERATING)}$	1.75	2	2.25	V
VCG Shunt regulator current	$I_{VCG(SREG)}$	5	V_{VCG}=$VCG_{(DISABLED)}$ – 100mV, V_{VDD}=12V	-	12	26	uA
VCG Shunt Load Regulation	$\Delta VCG_{(SREG)}$	5	26uA<I_{VCG}≤ 5mA, I_{FB}=350uA	-	125	200	mV
VCG LDO regulation voltage	$VCG_{(LREG)}$	5	V_{VDD}=20V, I_{VCG}=–2mA	-	13	-	V
VCG LDO Dropout voltage	$VCG_{(LREG, DO)}$	-	VDD–VCG, V_{VDD}=11V, I_{VCG}=–2mA	-	2	2.8	V
UVLO Turn-on threshold voltage	$VDD_{(ON)}$	8		9.7	10.2	10.7	V
UVLO Turn-off threshold voltage	$VDD_{(OFF)}$	8		7.55	8	8.5	V
UVLO hysteresis	$\Delta VDD_{(UVLO)}$	8	$VDD_{(ON)}$ – $VDD_{(OFF)}$	1.9	2.2	2.5	V
VDD switch on-resistance	$R_{DS, ON(VDD)}$	6,8	V_{VCG}=12V, V_{VDD}=7V, I_{DRN}=50mA *	-	4	10	Ω
Fault Latch Reset VDD voltage	$VDD_{(FAULT RESET)}$	8		5.6	6	6.4	V

*Standard design value

(Ta = 25°C, V_{VDD} = 12V)

Parameter	Symbol	Pin No.	Condition	MIN	TYP	MAX	Unit
2. MODULATION							
Minimum switching period	$t_{SW(HF)}$	6	FM mode I_{FB}=5uA	7.53	8.10	8.67	us
Maximum switching period	$t_{SW(LF)}$	6	$I_{FB}=I_{FB,\ CNR3}$ – 20uA	32.4	36.0	39.6	us
DRN maximum peak current	$I_{DRN(peak,\ max)}$	6	I_{FB}=5uA, R_{PCL}=33.2kΩ *	TBD	3	TBD	A
		6	I_{FB}=5uA, R_{PCL}=100kΩ *	TBD	1.0	TBD	A
DRN minimum peak current	$I_{DRN(peak,\ min)}$	6	$I_{FB,\ CNR2}$ +10uA, R_{PCL}=33.2kΩ *	TBD	1.0	TBD	A
		6	$I_{FB,\ CNR2}$ +10uA, R_{PCL}=100kΩ *	TBD	0.33	TBD	A
Minimum peak current	$I_{DRN(peak,\ absmin)}$	6	R_{PCL}=OPEN *	TBD	0.45	TBD	A
ILIM blanking time	$t_{BLANK(ILIM)}$	6	I_{FB}=5uA, R_{PCL}=100kΩ, 1.2A pull-up on DRN *	-	220	-	ns
PCL voltage	V_{PCL}	3	I_{FB}=5uA	2.94	3	3.06	V
		3	I_{FB}=230uA	0.95	1	1.05	V
I_{FB} range for FM mode	$I_{FB,\ CNR1}$	1	$t_S=t_{S(LF)}$, $I_{DRN}=I_{DRN(peak,\ max)}$	145	165	195	uA
I_{FB} range for AM mode	$I_{FB,CNR2}$ – $I_{FB,CNR1}$	1	$t_S=t_{S(LF)}$, $I_{DRN(peak)}$ variation range = $I_{DRN(peak,\ max)}$ ~ $I_{DRN(peak,\ min)}$	35	45	65	uA
I_{FB} range for LPM	$I_{FB,CNR3}$ – $I_{FB,CNR2}$	1		50	70	90	uA
I_{FB} hysteresis for LPM	$I_{FB,\ LPM-HYST}$	1		10	25	40	uA
FB voltage	V_{FB}	1	I_{FB}=10uA	0.34	0.7	0.84	V
3. DRIVER							
Driver on-resistance	$R_{DS(on)(DRN)}$	6,7	I_{DRN}=4.0A *	-	200	400	mΩ
Driver off leakage current	$I_{DRN(OFF)}$	6,7	V_{DRN}=12V	-	1.5	20	uA
High-side driver on-resistance	$R_{DS(on)(HS-DRV)}$	5,6	I_{DRN}=-50mA *	-	6	11	Ω
DRN discharge current	$I_{DRN,DSCH}$	6,7	VDD=OPEN, DRN=12V, Fault latch set	2.38	3.40	4.42	mA

*Standard design value

(Ta = 25°C, V_{VDD} = 12V)

Parameter	Symbol	Pin No.	Condition	MIN	TYP	MAX	Unit
4. TRANSFORMER ZERO ENERGY DETECTION							
TZE zero crossing threshold voltage	$V_{TZE(TH)}$	2	*	5	20	50	mV
TZE clamp voltage	$V_{TZE(CLAMP)}$	2	I_{TZE}=–10uA	-200	-160	-100	mV
Start timer operation threshold voltage	$V_{TZE(START)}$	2		0.1	0.15	0.2	V
Driver turn-on Delay time	$t_{DRY(TZE)}$	6	150Ω pull-up 12V on DRN	-	150	-	ns
Wait time for zero energy detection	$t_{WAIT(TZE)}$	6		2	2.4	2.8	
Start timer period	t_{ST}	6	V_{TZE}=0V	150	240	300	us
5. OVERVOLTAGE FAULT							
OVP threshold voltage	$V_{TZE(OVP)}$	2		4.85	5	5.15	V
OVP blanking time	$t_{BLANK, OVP}$	6		0.6	1	1.7	us
Input bias current	$I_{TZE(bias)}$	2	V_{TZE}=5V	-0.1	0	0.1	uA
6. OVERLOAD FAULT							
Over Load detection current	$I_{FB(OL)}$	1	*	0	1.5	3	uA
Over Load delay time	t_{OL}	6	I_{FB}=0A	200	250	300	ms
Retry time after Over Load	t_{RETRY}	6	R_{OTM}=76kΩ	-	750	-	ms
Over Load detection boundary resistance	$R_{OTM(TH)}$	4		100	120	150	kΩ
7. SHUTDOWN THRESHOLD							
Shutdown Threshold voltage	$V_{OTM(Vth)}$	4	V_{OTM}=high to low	0.7	1	1.3	V
Shutdown OTM current	$I_{OTM, PU}$	4	V_{OTM}= $V_{OTM(vth)}$	-600	-450	-300	uA
8. MAXIMUM ON TIME							
ON-Time	t_{OTM}	6	R_{OTM}=383kΩ	3.43	3.83	4.23	us
		6	R_{OTM}=76kΩ	3.4	3.8	4.2	us
OTM voltage	V_{OTM}	4		2.7	3	3.3	V

* Standard design value

(Ta = 25°C, V_{VDD} = 12V)

Parameter	Symbol	Pin No.	Condition	MIN	TYP	MAX	Unit
9. OTP							
Protection temperature	T_{SD}	6	Tj, temperature rising*	-	150	-	°C
Protection temperature hysteresis	T_{SD_HYS}	6	Tj, temperature falling, degrees below T_{SD}*	-	25	-	°C
10. POWER SUPPLY CURRENT							
Power supply current	$I_{VDD(STATIC)}$	8	V_{VDD}=20V, V_{TZE}=1V	1.36	1.8	2.34	mA
	$I_{VDD(OPERA-TING)}$	8	V_{VDD}=20V *	-	3	3.7	mA
Power supply current for LPM	$I_{VDD(LPM)}$	8	I_{FB}=350uA	-	550	1050	uA
Power supply current for UVLO	$I_{VDD(UVLO)}$	8	V_{VDD}= $VDD_{(ON)}$ – 100mV	-	285	500	uA

*Standard design value

■ FUNCTION EXPLANATION

(1) LED Current Control Function

MB39C601 is a flyback type switching regulator controller. The LED current is regulated by controlling the switching on-time or controlling the switching frequency depending on the LED load.The LED current is converted into detecting voltage (Vs) by sense resistor (Rs) connected in series with LED. Vs is compared by an external error amplifier (Err AMP).When Vs falls below a reference voltage, Err AMP output rises and the current that flows into the Opto-Coupler is decreased.

The OTM pin current is controlled via the Opto-Coupler in the on-time control block. In on-time control, it controls on-time at OTM pin current. So, on-time increases when the current of OTM pin decreases. And the average current supplied to LED is regulated, because on-time is regulated at the constant switching frequency.

The FB pin current is controlled via the Opto-Coupler in the switching frequency control block. In switching frequency control, it controls switching frequency at FB pin current. So, switching frequency becomes high when the current of FB pin decreases. And the average current supplied to LED is regulated, because switching frequency is regulated at the constant on-time.

(2) Cascode Switching

The switch in Primary Winding is a cascode connection.The gate of external MOSFET is connected with the VCG pin, and the source is connected with the drain of internal Driver MOSFET. When the swich is on-state, internal Driver MOSFET is turned on, internal HS Driver MOSFET is turned off, and the source voltage of external MOSFET goes down to GND. For this period the DC bias is supplied to the gate of external MOSFET from VCG pin. Therefore external MOSFET is turned on.

When the switch is off-state, internal Driver MOSFET is turned off, HS Driver MOSFET is turned on, and the source voltage of external MOSFET goes up to VCG voltage. For this period the DC bias is supplied to the gate of external MOSFET from VCG pin. Therefore external MOSFET is turned off. Moreover, the current flowing into internal Driver MOSFET is equal to the current of Primary Winding. Therefore, the peak current into Primary Winding can be detected without the sense resistor.

(3) Natural PFC (Power Factor Correction) Function

In the AC voltage input, when the input current waveform is brought close to the sine-wave, and the phase difference is brought close to Zero, Power Factor is improved. In the flyback method operating in discontinuous conduction mode, when the input capacitance is set small, the input current almost becomes equal with peak current of Primary Winding.

$$I_{PEAK} = \left(\frac{V_{BULK} \times t_{ON}}{L_{MP}} \right) = \left(\frac{V_{BULK}}{\left(\frac{L_{MP}}{t_{ON}} \right)} \right)$$

V_{BULK} : Supply voltage of Primary Winding
L_{MP} : Inductance of Primary Winding
t_{ON} : On-time

In on-time control, if loop response of Error Amp. is set to lower than the AC frequency (1/10 of the AC frequency), on-time can be constant. Therefore, input current is proportional to input voltage, so Power Factor is regulated.

(4) Power-Up Sequencing

When the voltage is input to VBULK, the electric charge is charged to capacitance of the VCG pin (CVCG) through starting resistor (Rst). So, the voltage of the VCG pin rises. The voltage of the DRN pin rises by source follower when the voltage of the VCG pin reaches the threshold voltage of the external HVMOSFET.

The DRN pin is connected with the VDD pin through the internal VDD Switch, and VDD capacitor (CVDD) is charged from the DRN pin. When the voltage at the VDD pin reaches the threshold voltage of UVLO, the VDD Switch is turned off, and the internal Bias circuit operates, and the switching is started.

After the switching begins, the voltage at the VDD pin is supplied from Auxiliary Winding through the external diode (DBIAS). The voltage of an Auxiliary Winding is decided by rolling number ratio of Auxiliary Winding and Secondary Winding, and the voltage of Secondary Winding. Therefore, the voltage at the VDD pin is not supplied, until the voltage of Auxiliary Winding rises more than the voltage at the VDD pin. In this period, it is necessary to set the capacitor of the VDD pin to prevent the voltage of the VDD pin from falling below the threshold voltage of UVLO.

The external Schottky diode (D1) is required between the DRN pin and VDD pin. This diode is used to prevent the current that flows through the body diode of the VDD Switch.

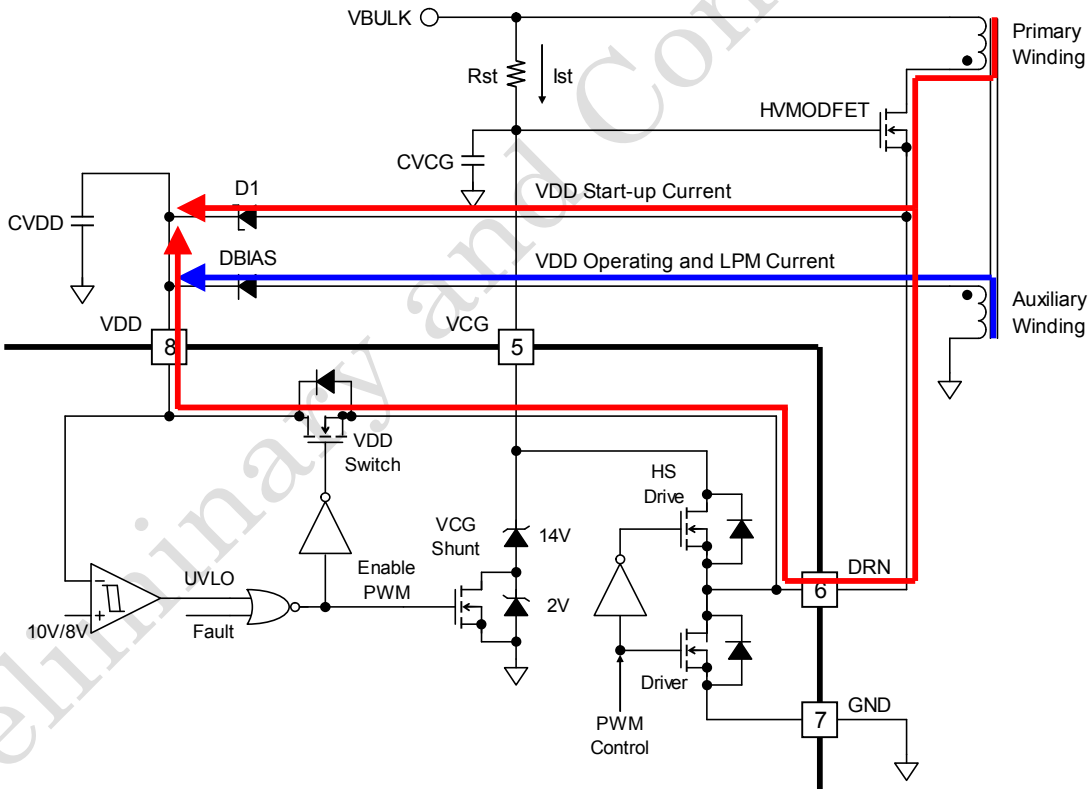


Figure 1 Current Passing When Starting

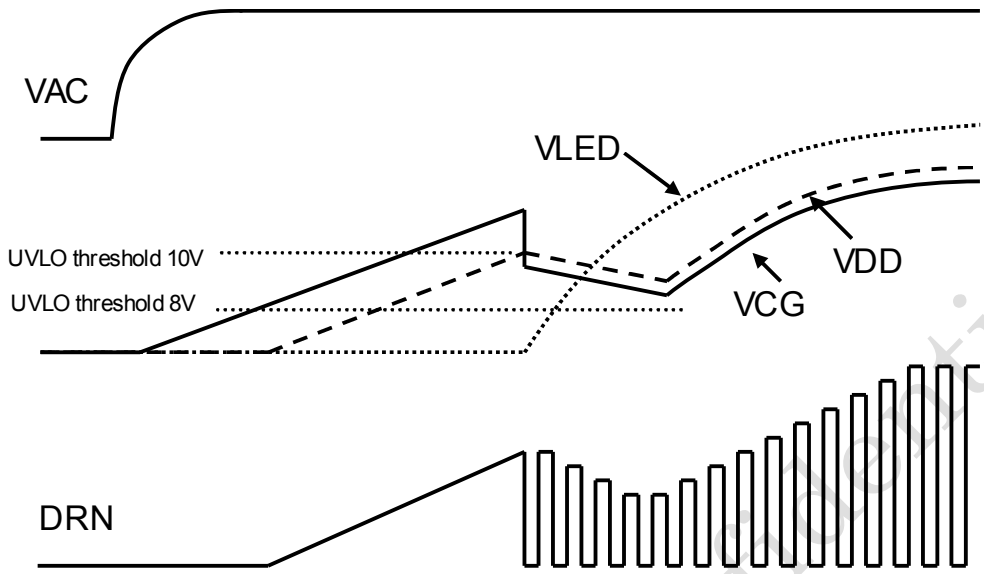


Figure 2 Power Up Sequencing

(5) Power Down Sequencing

When AC power is removed from the AC line, the current does not flow to Secondary Winding even if HV MOSFET is switching. The LED current is supplied from the output capacitance and decreases gradually. Similarly, the voltage at the VDD pin decreases because the current does not flow into Auxiliary Winding. The switching stops and MB39C601 becomes shutdown when the voltage at the VDD pin falls below the threshold voltage of UVLO.

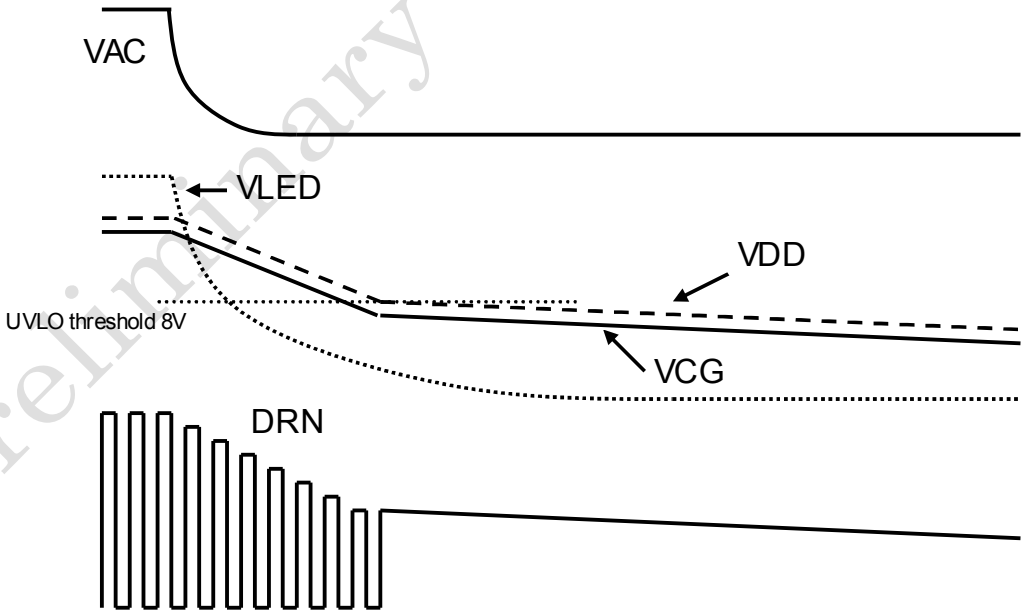


Figure 3 Power Down Sequencing

(6) OTM Part

It is set on-time by connecting resistance (R_{OTM}) with OTM pin.

As shown in following figure, the on-time can be controlled by connecting the collector of the Opto-Coupler through resistor from OTM.

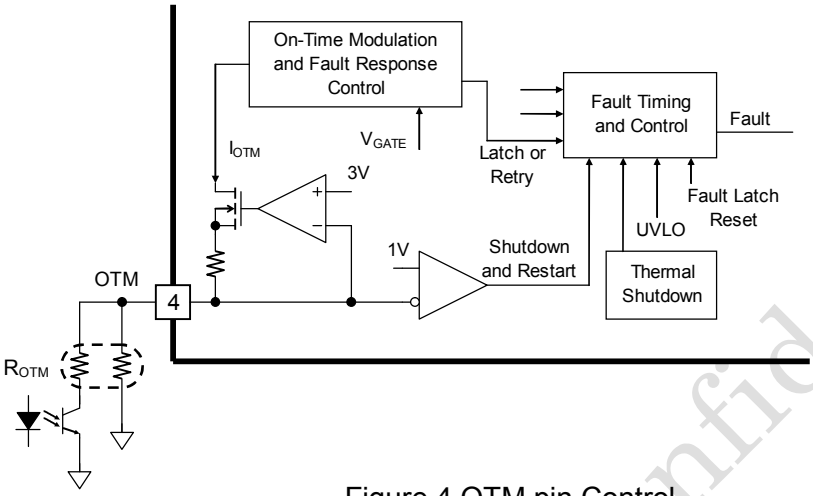


Figure 4 OTM pin Control

The following figure shows how the on-time is programmed over the range of between 1.5 μ s and 5 μ s for either range of programming resistors. The resistor range determines the controller response to a sustained overload fault (to either latch-off or to shutdown/retry). See the item of the overload protection about details of "latch-off" and "shutdown/retry". On-time is related to the programmed resistor based on the following equations.

$$(1) \quad R_{OTM} = t_{OTM} \times \left(2 \times 10^{10} \frac{\Omega}{S} \right)$$

$$(2) \quad R_{OTM} = t_{OTM} \times \left(1 \times 10^{11} \frac{\Omega}{S} \right)$$

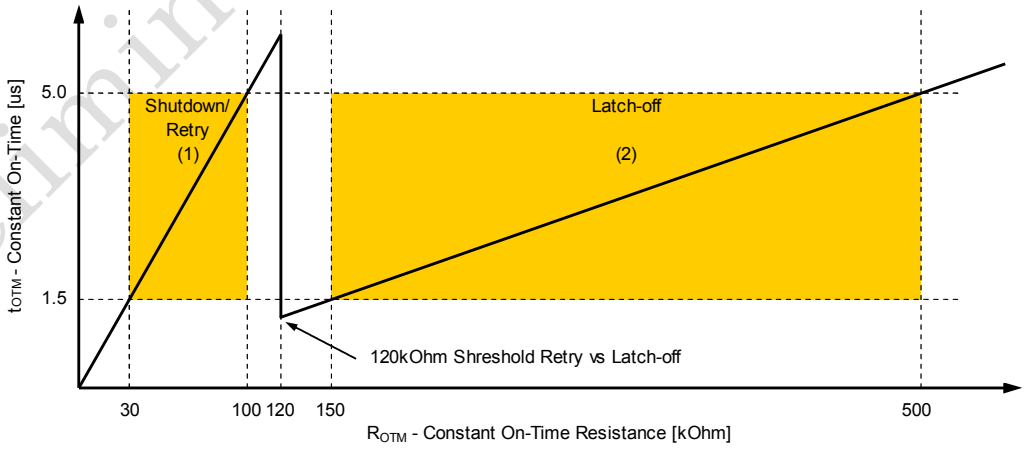


Figure 5 On-time Setting Range

Moreover, it can be shutted down by making the voltage of OTM pin below "$V_{OTM(Vth)}$ (typ1V)".

(7) PCL Part

It is set the peak current of Primary Winding by connecting resistance with PCL pin.

The maximum peak current of Primary Side is set by connecting resistance (R_{PCL}) between the PCL pin and GND.

$$I_{DRN(pk)} = \left(\frac{100kV}{R_{PCL}} \right)$$

An about 220ns blanking time of the beginning of switching cycle is masking the spike noise. As a result, it prevents the sense of current from malfunctioning (See the figure below.).

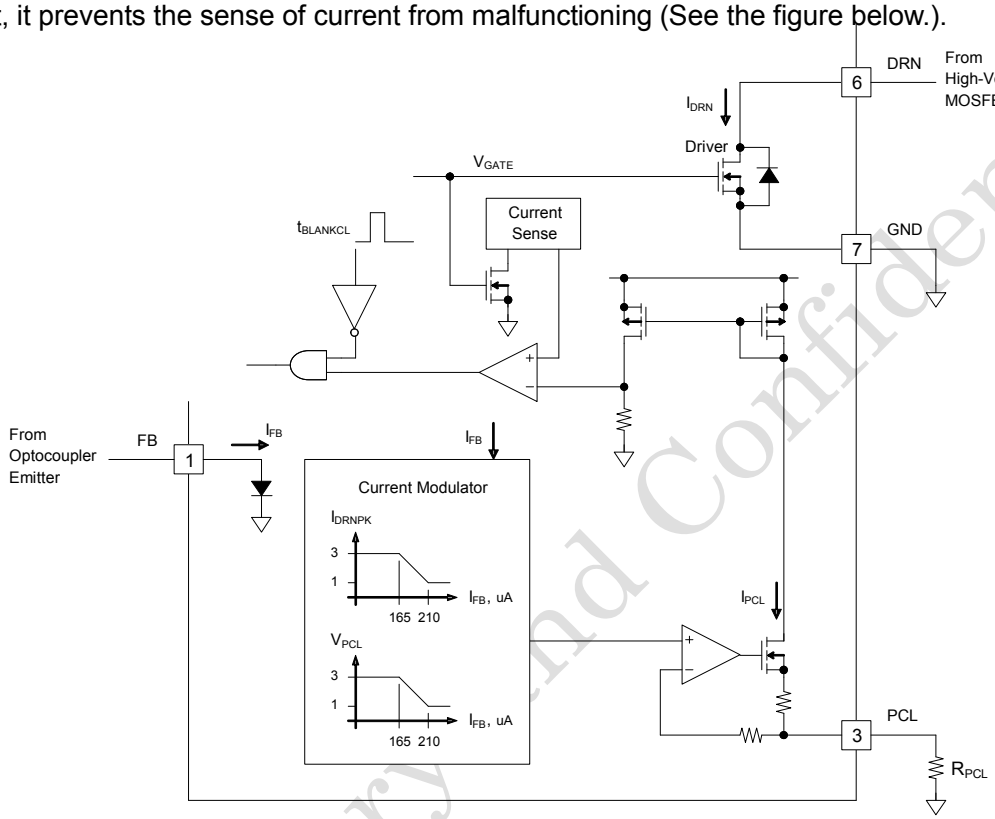


Figure 6 Peak Current Control with PCL pin

(8) FB Part

The switching frequency is controlled by setting the current of the FB pin. In on-time control, the switching frequency is set by pulling up the FB pin to VDD through resistance.

Moreover, as shown in following figure, it is possible to control the switching frequency by connecting the emitter of the Opto-Coupler from the FB pin through resistor. Resistor (R_{FB}) is connected to bleed off the dark current of Opto-Coupler.

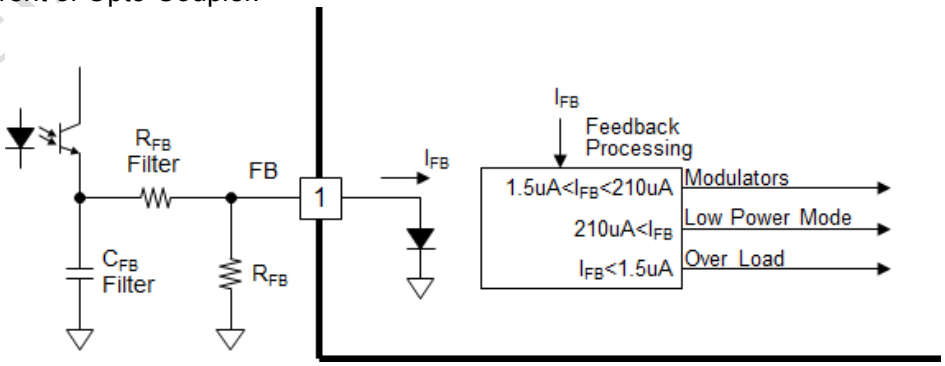


Figure 7 FB pin Control

MB39C601 becomes the following three modes by FB current (I_{FB}).

1. Frequency Modulation Mode (FM)
   The peak current of HV-MOSFET is set to the maximum, and the LED current is regulated by adjusting the switching frequency with I_{FB}.The range of the switching frequency is from 30 kHz to 130 kHz. Maximum peak current $I_{DRN\ (peak,\ max)}$ of HV-MOSFET is set by the resistance of the PCL pin.
2. Amplitude Modulation Mode (AM)
   The LED current is regulated by adjusting the peak current of HV-MOSFET with I_{FB}.The switching frequency is about 30 kHz. And the range of HV-MOSFET of the peak current is from 33% to 100% of the maximum. Maximum peak current $I_{DRN\ (peak,\ max)}$ of HV-MOSFET is set by the resistance of the PCL pin.
3. Low Power Mode (LPM)
   MB39C601 becomes two states of LPM-ON and LPM-OFF at a light load. In the LPM-ON mode, it is operated at 30 kHz switching frequency. And the current is supplied to LED. At this time, the feedback current from the Opto-Coupler increases, and it changes to the LPM-OFF mode. In the LPM-OFF mode, it is not operated. And the current is supplied to LED from Co. When the feedback current from the Opto-Coupler decreases, it changes to the LPM-ON mode. LED is lit by the power saving repeating these two states.
   Three modes of the FM, AM, and LPM change depending on the load of LED. At the light load, three modes change from FM to AM to LPM.

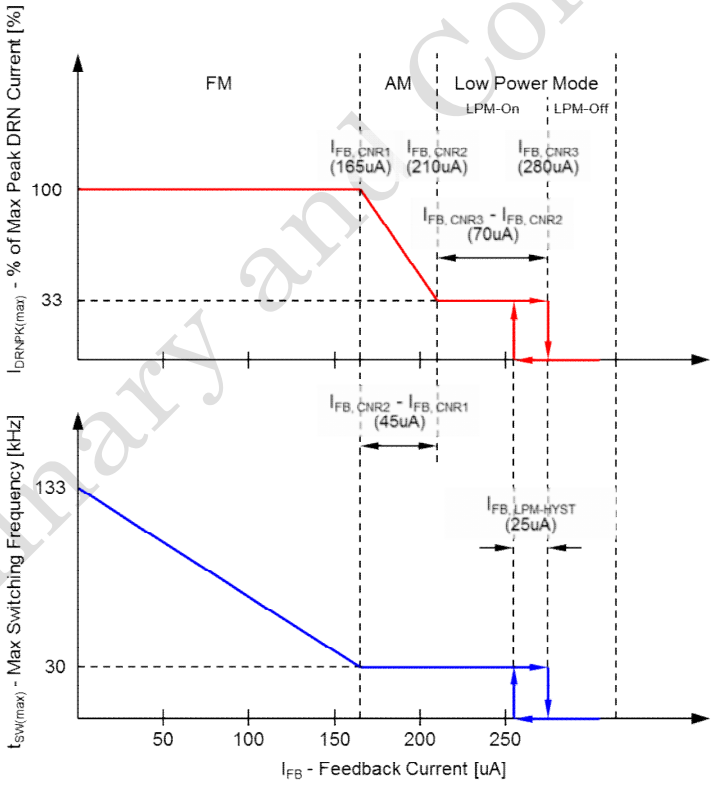


Figure 8 Switching Frequency and Peak Current Control Operation Based On FB pin

(9) TZE Part

MB39C601 requires the following three conditions in order to start the next switching cycle.

1. The time since the last turn-on edge must be equal to or longer than the switching time set by I_{FB}.
2. The time since the last turn-on edge must be longer than the minimum switching period set by MB39C601 (nominally 7.5us which equals 133kHz).
3. Immediately after zero energy detection at TZE pin. Or, the time since the last zero energy detection must be longer than $t_{WAIT,TZE}$ (2.4us or less) .

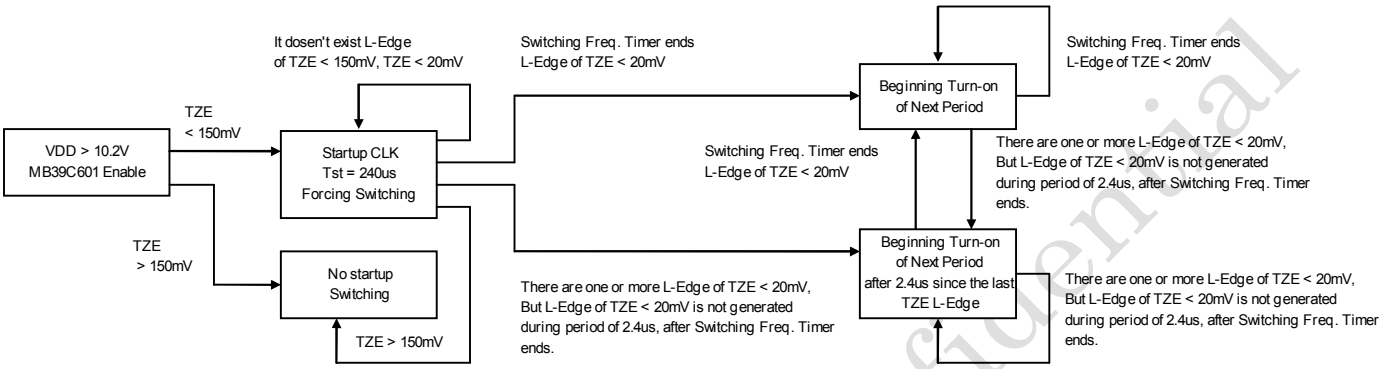


Figure 9 Starting switching cycle diagram

The TZE pin is connected with Auxiliary Winding of the transformer through the resistance division, and detects zero energy as shown below.

A delay, 50ns to 200ns, can be added with C_{TZE} to adjust the turn-on of the primary switch with the resonant bottom of Primarty Winding waveform.

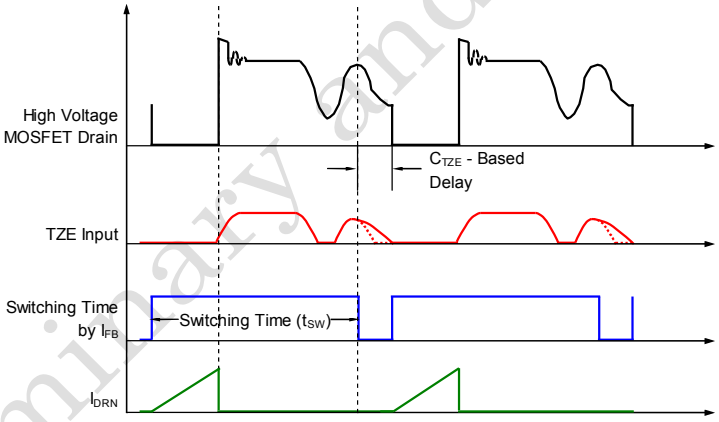


Figure 10 Switching Waveform at detecting zero Energy

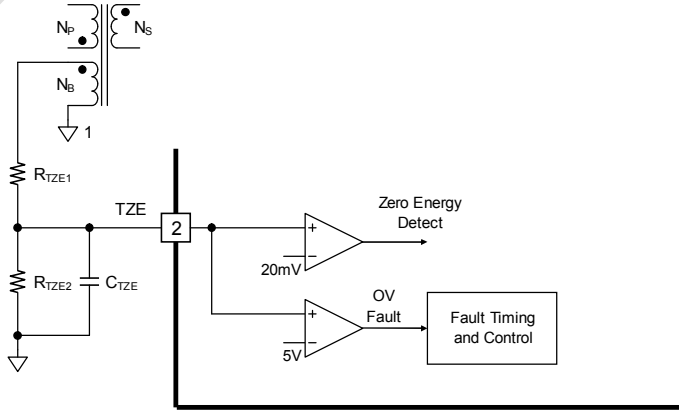


Figure 11 TZE pin Connection

■ VARIOUS PROTECTION CIRCUITS

Under voltage lockout protection (UVLO)

The under voltage lockout protection (UVLO) protects IC from malfunction and protects the system from destruction/deterioration during the transient state and momentary drop due to start up for the power supply pin voltage (VDD). The voltage decrease of the VDD pin is detected with comparator, and output HS DRIVER is turned off and output DRIVER is turned off, and the switching is stopped.The system returns if the VDD pin becomes more than the threshold voltage of the UVLO circuit.

Over voltage Proteciton(OVP)

When LED is in the state of open and the output voltage rises too much, the voltage of Auxiliary Winding and the voltage of the TZE pin rise. The over voltage is detected by sampling this voltage of the TZE pin.
When TZE pin voltage rises more than the threshold voltage of OVP, the over voltage is detected. Output HS DRIVER is turned off, and output DRIVER is turned off, and the switching is stopped. (latch-off)

If the VDD pin becomes below the voltage of Fault Latch Reset, OVP is released.

Over load protection (OL)

When the cathode or the anode of LED is short to GND and it becomes an overloaded status at switching frequency control, the current does not flow into Rs and there is no current feedback to I_{FB}. The current of FB pin detects the overload with 1.5μA or less. OL state is decided to latch-off or shutdown/retry by R_{OTM}.

Shutdown/retry … MB39C601 becomes two states of switching on for 250ms and switching off for 750ms. These states are repeated. If it is not OL status, it returns.

Latch-off … The switching is continued for 250ms. If it does not return from OL states for this period, output HS DRIVER is turned off, and output DRIVER is turned off, and the switching is stopped. If it returns from OL states after this time and the switching is still stopped (latch-off) and the VDD pin becomes below the voltage of Fault Latch Reset, Latch is released.

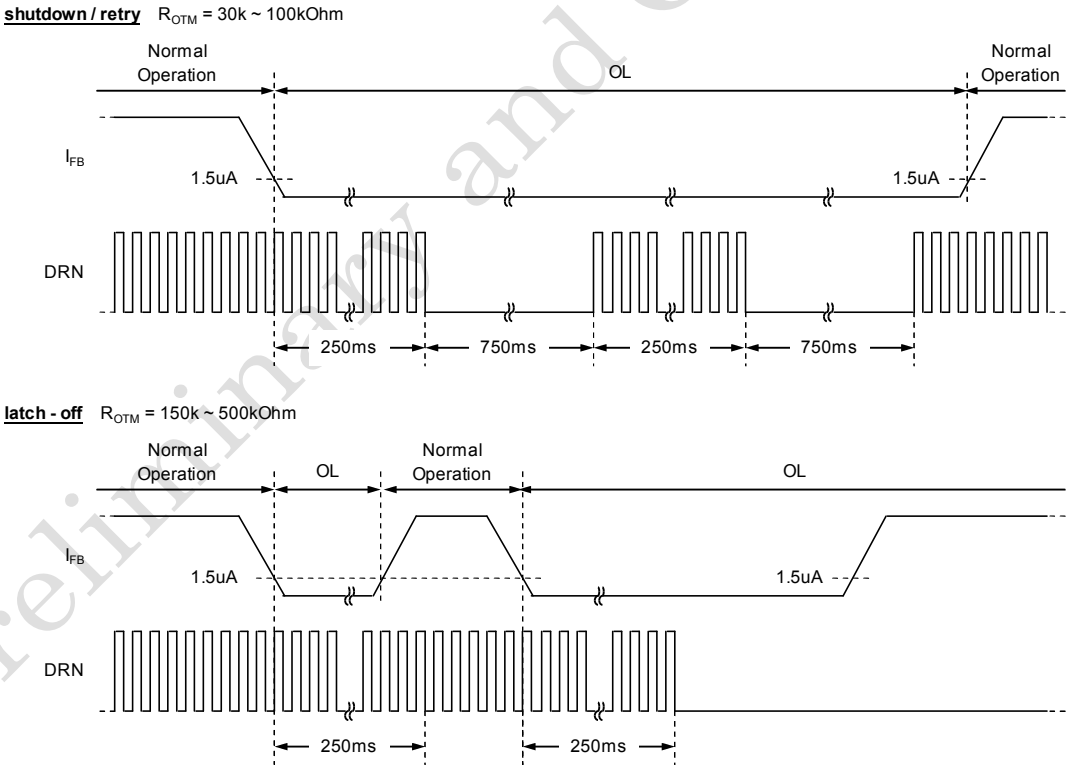
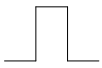
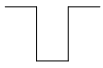
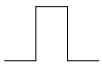
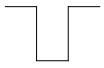


Figure 12 Over Load Protection Sequencing

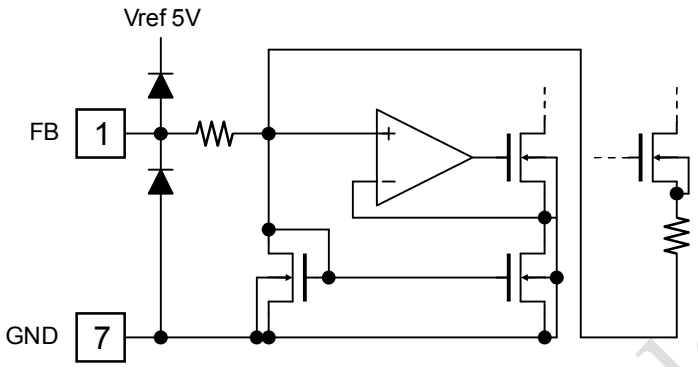
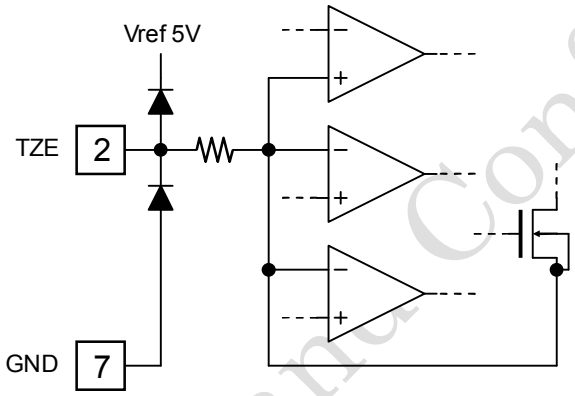
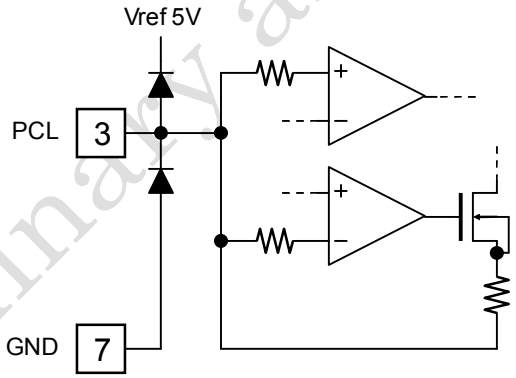
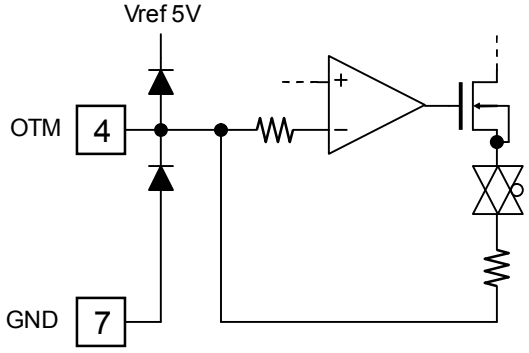
Over temperature protection (OTP)

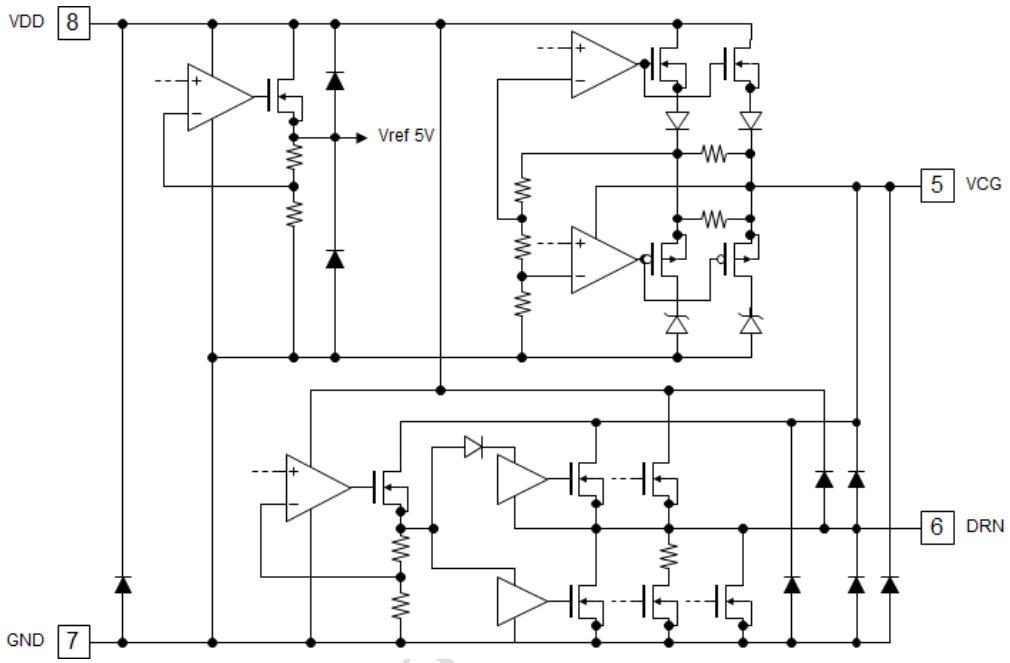
The over temperature protection (OTP) is a function to protect IC from the thermal destruction.When the junction temperature reaches +150°C,output HS DRIVER is turn off, and output DRIVER is turned off, and the switching is stopped.It returns again when the junction temperature falls to +125°C (automatic recovery).

■ Various Function Tables

Function		DRN				Detection Condition at Protected Operation	Return Condition	Remarks
		LS_DRV	HS_DRV	VDD SW	Discharge SW			
Normal Operation				OFF	OFF	-	-	-
Under Voltage Lockout Protection (UVLO)		OFF	OFF	ON	OFF	VDD < 8.0V	VDD > 10.2V	Standby
OTM Shutdown		OFF	OFF	ON	OFF	OTM = GND	OTM > 1V	Standby
Over Voltage Protection (OVP)		OFF	OFF	ON	ON	TZE > 5V	VDD < 6V ---> VDD > 10.2V	Latch - off
Over Load Protection (OL)	Shutdown / Retry Mode			OFF	OFF	I_{FB} < 1.5uA 30k < R_{OTM} < 100kOhm	I_{FB} > 1.5uA	Shutdown Retry OL Timer (250ms)
		OFF	OFF	ON	OFF			Shutdown Retry Fault (750ms)
	Latch - Off Mode	OFF	OFF	ON	ON	I_{FB} < 1.5uA 150k < R_{OTM} < 500kOhm	VDD < 6V ---> VDD > 10.2V	Latch-off
Stopped state of Low Power Mode		OFF	OFF	ON	OFF	I_{FB} > 275uA	I_{FB} < 255uA	-
Over Temperature Protection (OTP)		OFF	OFF	ON	OFF	Tj > 150°C	Tj < 125°C	-

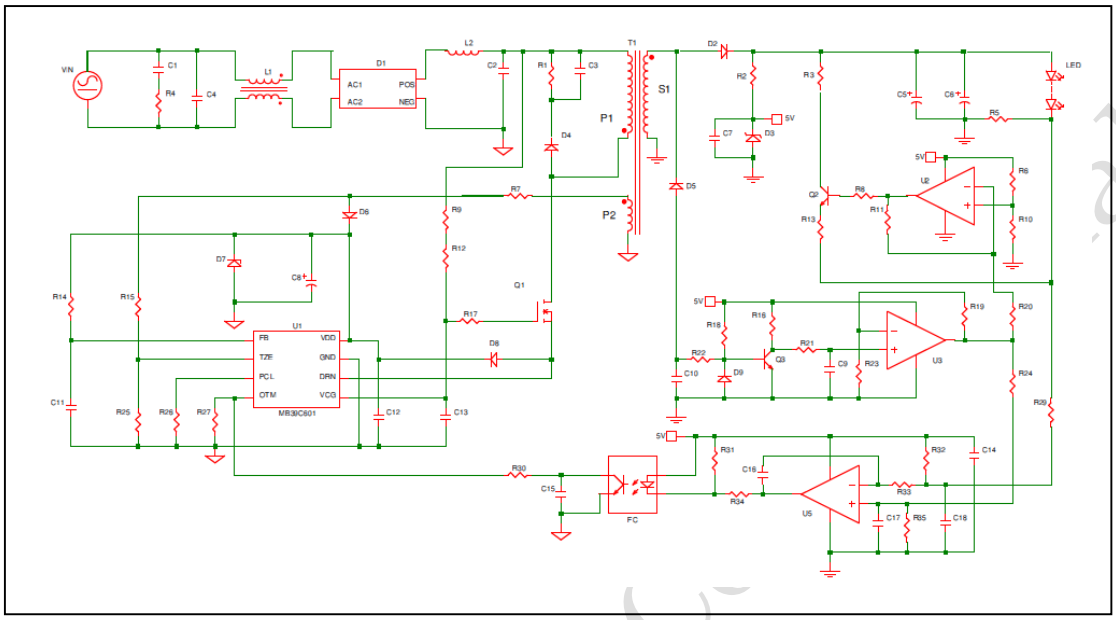
■ Input / Output pin equivalent circuit schematic

Pin Name	Equivalent Circuit Schematic
1pin : FB	
2pin : TZE	
3pin : PCL	
4pin : OTM	

Pin Name	Equivalent Circuit Schematic
5pin : VCG 6pin : DRN	

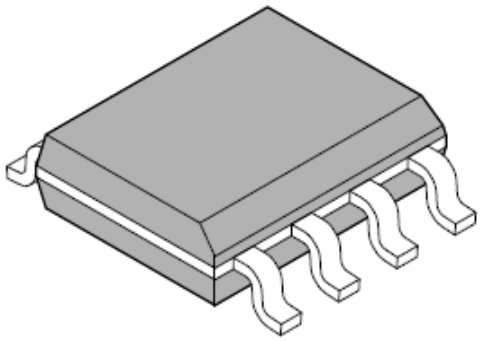
■ Application example

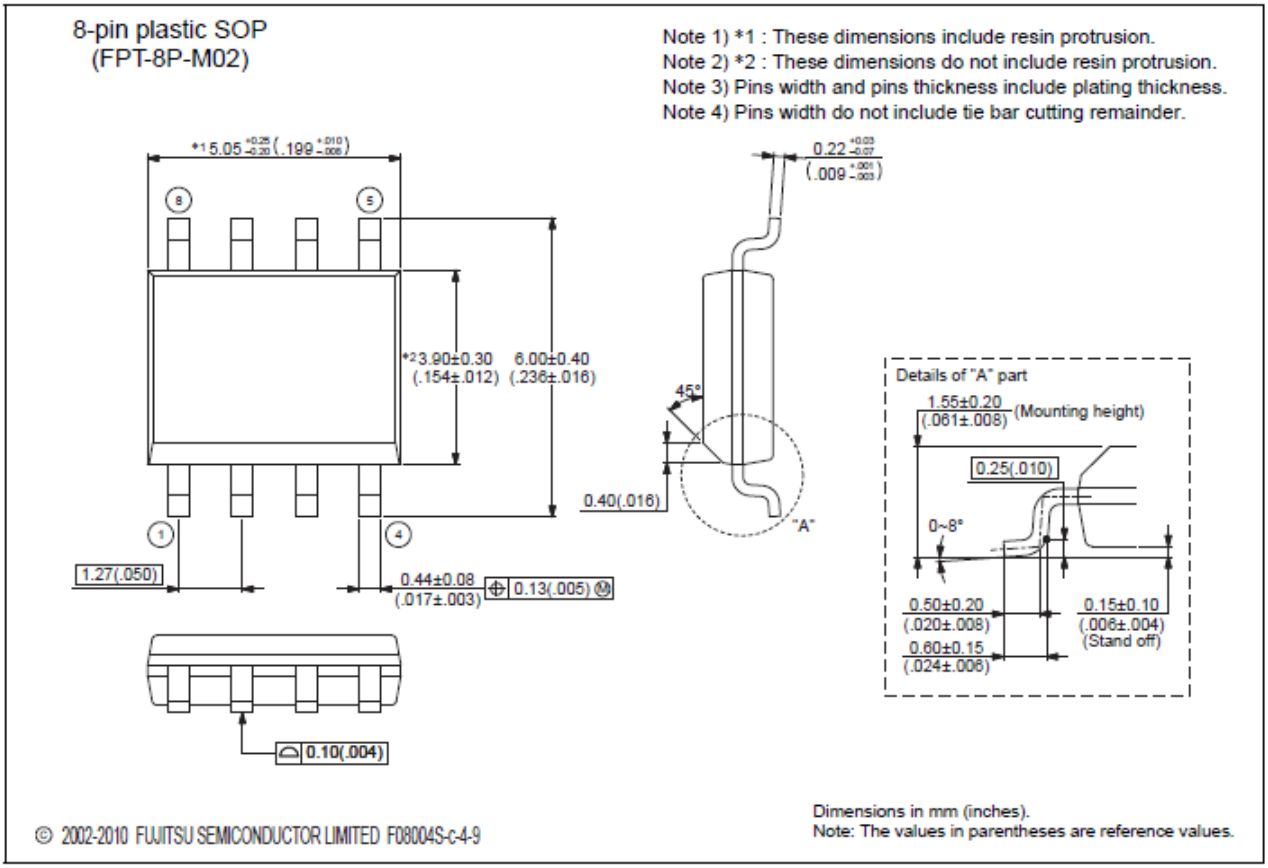
Triac dimmable circuit



■ PACKAGE DIMENSIONS

FPT-8P-M02

8-pin plastic SOP		
	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g
(FPT-8P-M02)		



◆ USAGE PRECAUTION

1. Do not configure the IC over the maximum ratings.
If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

2. Use the device within the recommended operating conditions.
The recommended values guarantee the normal LSI operation under the recommended operating conditions. The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed circuit board ground lines should be set up with consideration for common impedance.

4. Take appropriate measures against static electricity.
- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

5. Do not apply negative voltages.
The use of negative voltages below - 0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

FUJITSU SEMICONDUCTOR LIMITED
Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858