REVISION HISTORY

Revision	Description	Issue Date
Rev. 0.1	Initial Issue	Oct. 26. 2007
Rev. 0.2	Modify Package Outline Dimension	Jan. 12. 2008
Rev. 1.0	Release Datasheet	Mar. 27. 2008
Rev. 1.1	Modify TSSOP package type R to A and I	Oct. 29. 2008

2.5 W/CH Stereo Class D Audio power Amplifier (TSSOP)

FEATURES

- 2.5 W/CH Into 4Ω from 5V power supply at THD = 10% (Typ.).
- 2.5V~5.5V Power supply.
- Low shutdown Current.
- Low Quiescent Current.
- Minimum external components.
- No output filter required for inductive loads.
- Output Pin Short-Circuit Protection (Short to Output Pin, Short to GND, Short to VCC)
- Low noise during turn-on and turn-off transitions.
- Lead free and green package available. (RoHS Compliant)
- TSSOP20 pin Packaging Available.

GENERAL DESCRIPTION

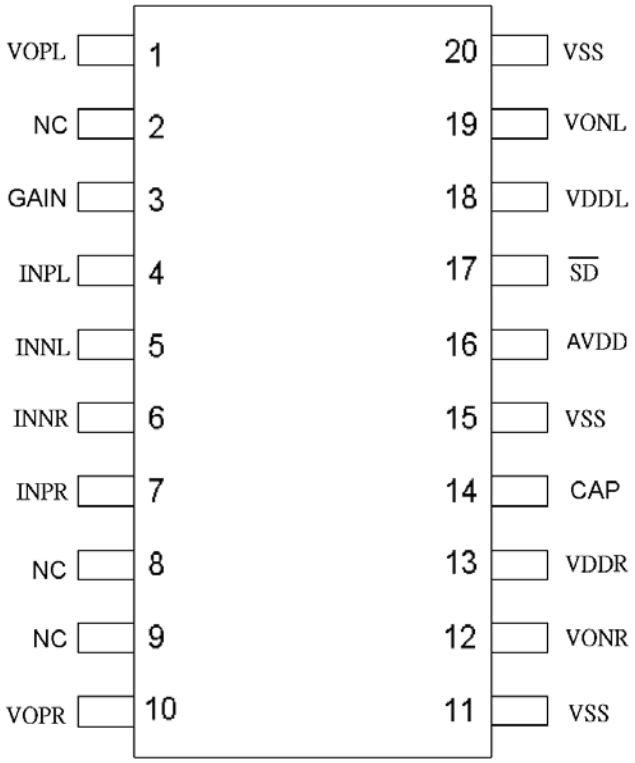
The LY8205 is a high efficiency, 2.5 W stereo class D audio power amplifier. It is a low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplify design.
The LY8205 is designed to meet of Multimedia application includes mobile phones and other portable electronic devices. The LY8205 is a single 5V supply, it is capable of driving 4Ω speaker load at a continuous average output of 2.5 W/CH (5W in all) with 10% THD+N or 8Ω speaker load at a continuous average output of 1.3 W/CH (2.5W in all) with 10% THD+N. Not external heat-sink is required. Output pin short circuit (short to output pin, short to ground and short to VDD) protection prevent the device from damage during fault conditions

APPLICATION

- Portable electronic devices.
- Mobile Phones, PDAs.
- DVD/CD Players, TFT LCD TVs/Monitors.
- USB Audio, 2.1 / 5.1 CH Audio System.

PIN CONFIGURATION

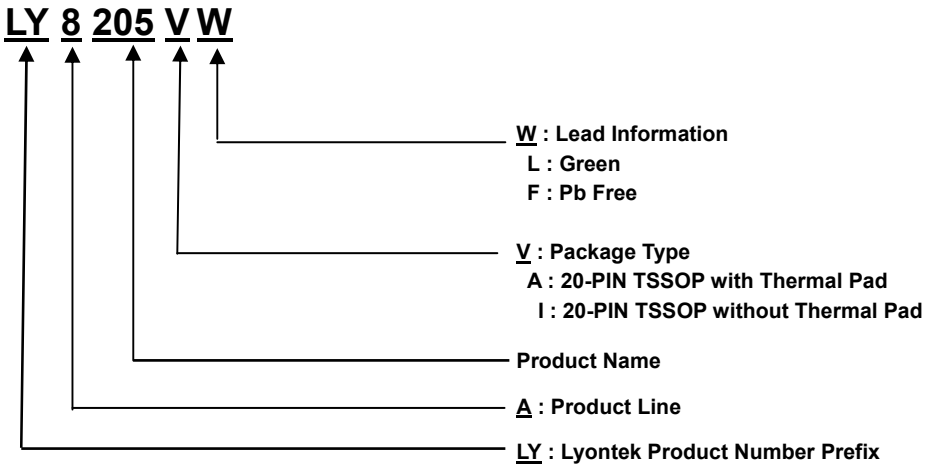
LY8205 TSSOP20 Pin Configuration (Top View)



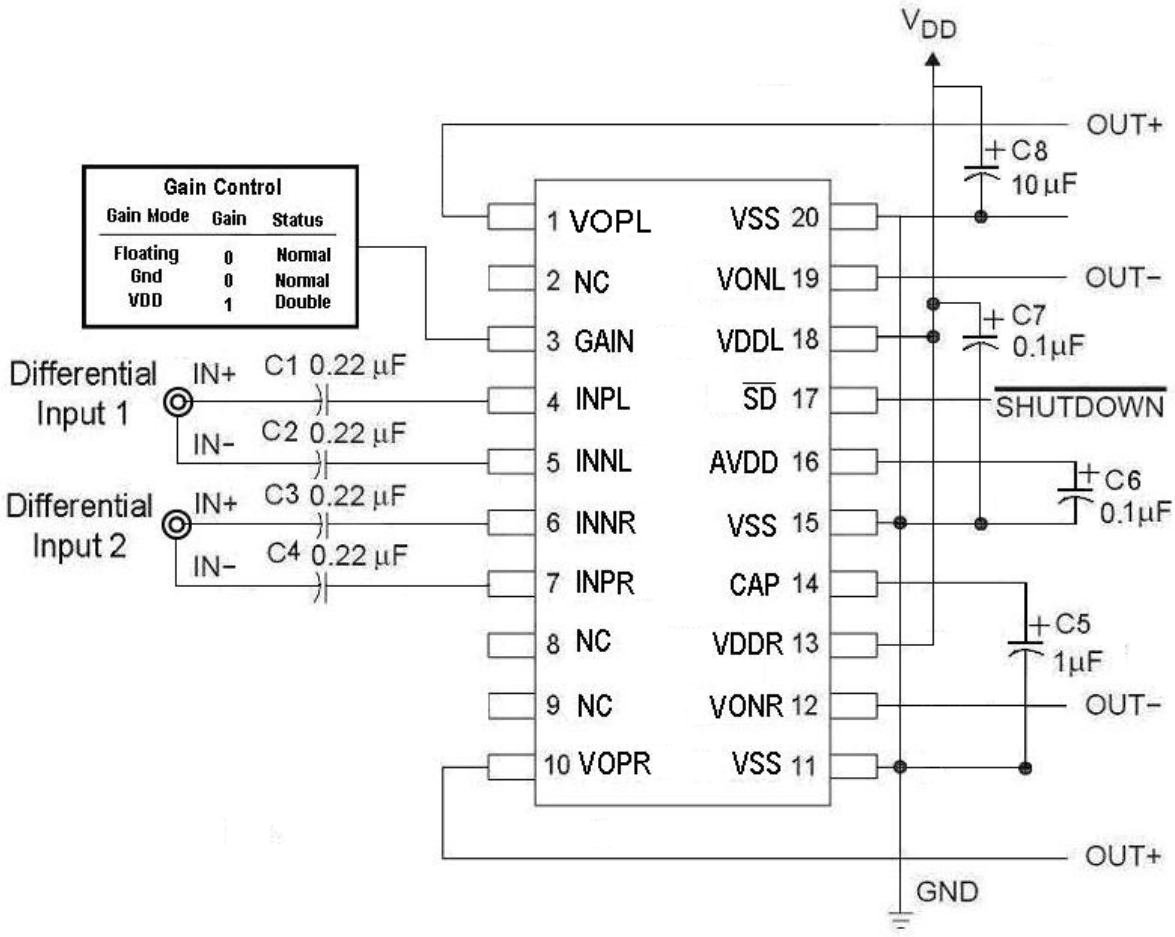
PIN DESCRIPTION

SYMBOL	Pin No.	DESCRIPTION
SD	17	Shutdown pin. (when low level is active the pin).
INPL	4	Positive input of left channel.
INNL	5	Negative input of left channel.
VOPL	1	Positive BTL output of left channel.
VONL	19	Negative BTL output of left channel.
V_{DD}L / V_{DD}R	13,18	Power supply
AV_{DD}	16	Analog Power supply
Vss	11,15, 20	Ground
INPR	7	Positive input of right channel.
INNR	6	Negative input of right channel.
VOPR	10	Positive BTL output of right channel.
VONR	12	Negative BTL output of right channel.
CAP	14	Capacitance for power up delay.
GAIN	3	Gain select
NC	2,8,9	No Connection.

ORDERING INFORMATION



Typical Application Circuit



ABSOLUTE MAXIMUN RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	6.0	V
Operating Temperature	T_A	0 to 70 (C grade)	°C
		-20 to 80 (E grade)	
		-40 to 85 (I grade)	
Input Voltage	V_I	-0.3V to V_{DD} +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	°C
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25℃,Unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output offset voltage (measured differentially)	$\|V_{OS}\|$	V_I = 0 V, Av = 2 V/V, V_{DD} = 2.5 V to 5.5 V	-	-	25	mV
High-level input current	$\|I_{IH}\|$	V_{DD} = 5.5 V, V_I = 5.8 V	-	-	100	uA
Low-level input current	$\|I_{IL}\|$	V_{DD} = 5.5 V, V_I = 0.3 V	-	-	5	uA
Power supply rejection ratio	PSRR	V_{DD} = 2.5 V to 5.5 V		-75	-55	dB
Common mode rejection ratio	CMRR	V_{DD}=2.5V to 5.5V, V_{IC}= V_{DD}/2 to 0.5 V, V_{IC}= V_{DD}/2 to V_{DD}-0.8 V,		-60	-48	dB
Quiescent Current / Ch	I_Q	V_{DD} = 5.5V, No Load	-	6.8	9.0	mA
		V_{DD} = 3.6V, No Load	-	5.6	-	
		V_{DD} = 2.5V, No Load	-	4.4	6.4	
Shutdown Current / Ch	I_{SD}	$V_{SHUTDOWN}$ = 0.8V, V_{DD} = 2.5V to 5.5V	-	0.6	4	μA

▪OPERATING CHARACTERISTICS (T_A = 25℃, Gain = 2V/V, R_L = 8Ω, Unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Out Power / Ch	P_O	THD+N= 10%, f = 1 kHz, R_L= 4Ω	V_{DD}=5V	-	2.5	-	W
			V_{DD}=3.6V	-	1.3	-	
			V_{DD}=2.5V	-	0.5	-	
		THD+N= 1%, f = 1 kHz, R_L= 4Ω	V_{DD}=5V	-	2.0	-	
			V_{DD}=3.6V	-	1.0	-	
			V_{DD}=2.5V	-	0.4	-	
		THD+N= 10%, f = 1 kHz, R_L= 8Ω	V_{DD}=5V	-	1.4	-	
			V_{DD}=3.6V	-	0.7	-	
			V_{DD}=2.5V	-	0.35	-	
		THD+N= 1%, f = 1 kHz, R_L= 8Ω	V_{DD}=5V	-	1.2	-	
			V_{DD}=3.6V	-	0.6	-	
			V_{DD}=2.5V	-	0.3	-	
Total harmonic distortion + noise	THD+N	P_O = 1 W, f = 1 kHz, R_L = 8Ω	V_{DD}=5V	-	0.15	-	%
		P_O = 0.5 W, f = 1 kHz, R_L = 8Ω	V_{DD}=3.6V	-	0.18	-	
		P_O = 0.2 W, f = 1 kHz, R_L = 8Ω	V_{DD}=2.5V	-	0.2	-	
Supply ripple rejection ratio	K_{SVR}	f = 217 Hz, V(RIPPLE) = 200mVpp, inputs ac-grounded with Ci = 2uF	V_{DD}=3.6V	-	-71	-	dB
Signal-to-noise ratio	SNR	P_O= 1 W, R_L = 8Ω	V_{DD}=5V	-	97	-	dB
Output voltage noise	Vn	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with Ci = 2 μF	No weighting	-	48	-	uV_{RMS}
			A weighting	-	36	-	
Common mode rejection ratio	CMRR	V_{IC} = 1 Vpp , f = 217 Hz	V_{DD}=3.6V	-	-63	-	dB
Start-up time from shutdown	Z_I	V_{DD} = 3.6 V		-	100	-	ms

Application Information Circuit

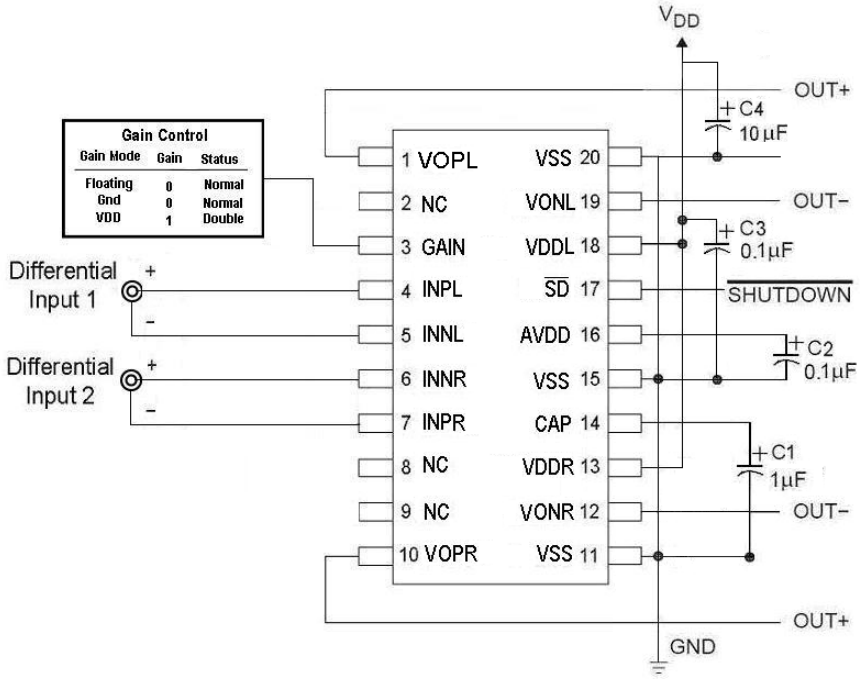


Figure 1. Application Schematic With Differential Input Configuration

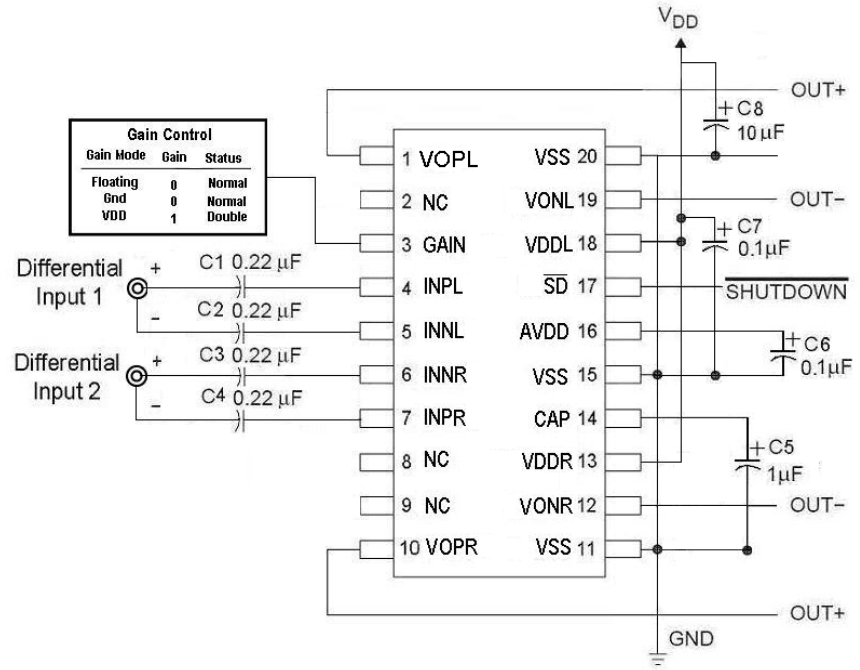


Figure 2. Application Schematic With Differential and Capacitors Input Configuration

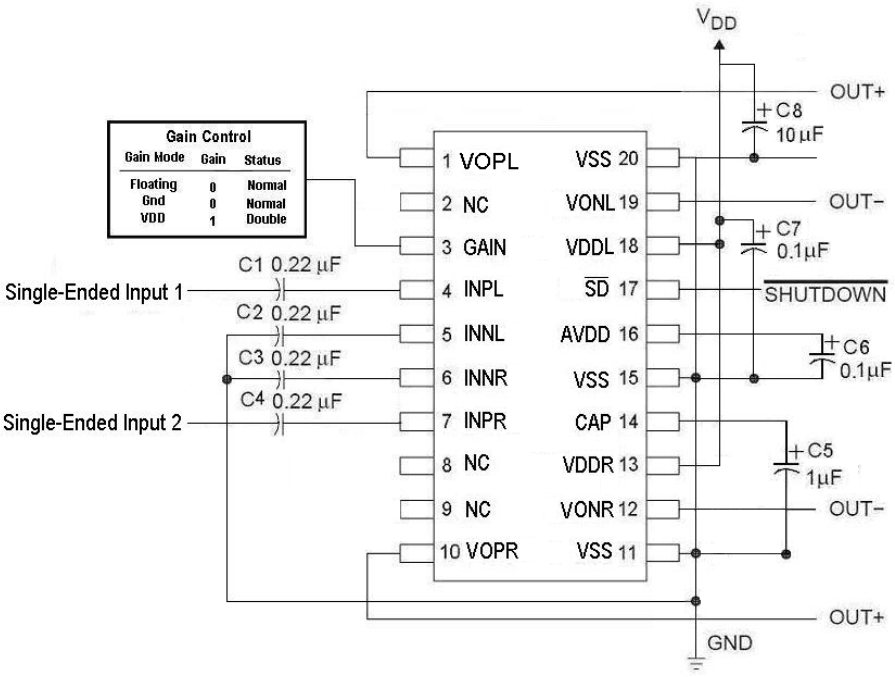


Figure 3. Application Schematic With Single-Ended Input

▪ APPLICATION INFORMATION

Fully Differential Amplifier

The LY8205 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential LY8205 can still be used with a single-ended input; however, the LY8205 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

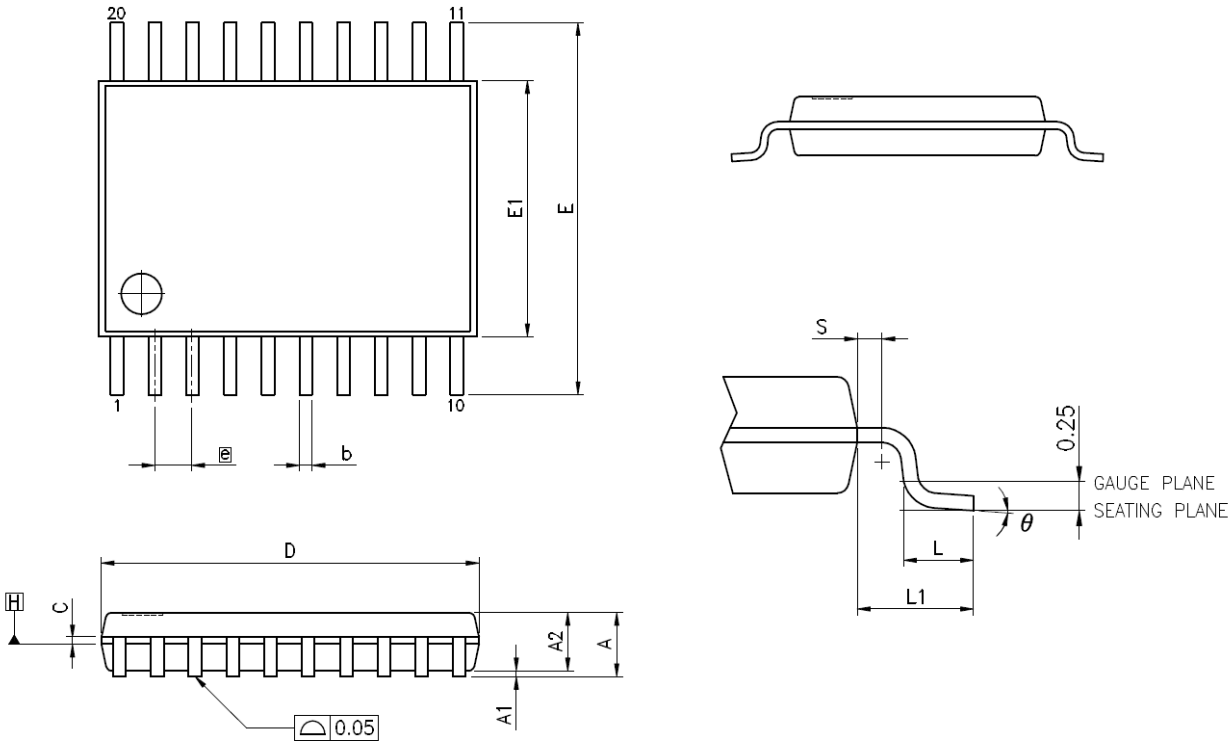
Input-coupling capacitors not required:
The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the LY8205, the common-mode feedback circuit will adjust, and the LY8205 outputs will still be biased at midsupply of the LY8205. The inputs of the LY8205 can be biased from 0.5 V to V_{DD} - 0.8 V. If the inputs are biased outside of that range, input - coupling capacitors are required.

Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.

Better RF-immunity:
GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

PACKAGE OUTLINE DIMENSION

20 Pin TSSOP Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	–	–
θ	0°	–	8°